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Thyristor Control of Electric Furnace Temperature

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Mullard Central Application Laboratory

Practical power control circuits for the automatic stabilisation of electric furnace temperatures are given for single-phase and three-phase operation. Current limit and surge suppression circuits are incorporated. The temperature stability attainable is limited only by the capabilities of the standard indicating temperature controller with which the circuits are used.

INTRODUCTION

The temperature of an electric furnace is generally required to be maintained within certain defined limits. This is achieved by sensing temperature deviations and feeding them back to a control system that makes appropriate adjustments to the power applied to the heating elements. The main functional blocks of a furnace control are shown in Fig. 1.

Temperature sensing is usually achieved by resistance thermometer, thermocouple, or radiation pyrometer.

The signal from the temperature sensor is fed into a temperature controller. This usually comprises a visual indicator of the temperature, a means of setting limits beyond which corrective action will be required, and a circuit that provides an output signal (usually 0 to 5mA into 2kΩ) to operate the power controller.

The power supplies of industrial ovens and furnaces have traditionally been controlled by electromechanical contactors. These devices, however, present problems of contact maintenance, especially where large powers are switched. It has become apparent that electronic methods of control would overcome this difficulty.

In addition, there has been an increasing demand for faster response and greater accuracy of control, with the added requirements of current limiting and overload protection.

In a number of installations this more exacting specification has been met by magnetic amplifiers; but, more recently, thyristors have been able to compete economically, with the advantages of smaller size and greater flexibility when temperature cycling is required.

The present article considers power controllers employing thyristors, their associated firing circuits, and current limit circuits.

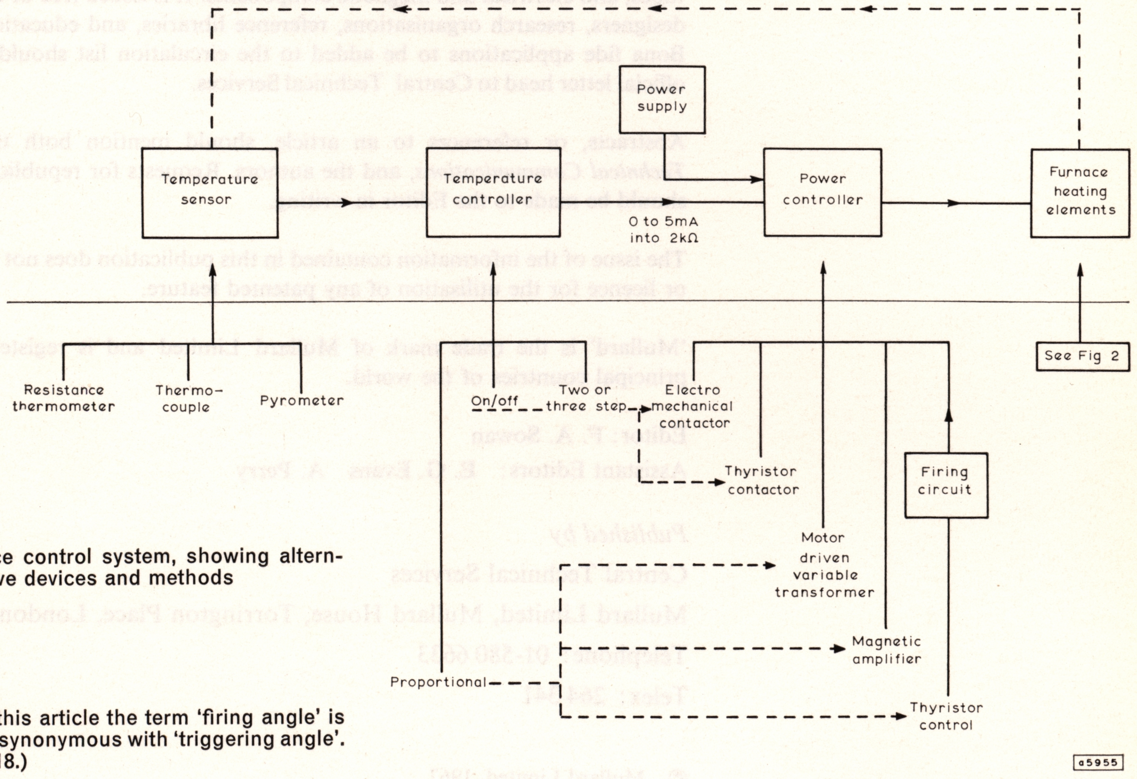


Fig. 1—Furnace control system, showing alternative devices and methods

Note: In this article the term 'firing angle' is used. It is synonymous with 'triggering angle'. (See Fig. 18.)

TYPES OF FURNACE CONTROL

The method used for the control of power into the furnace depends mainly on the accuracy of the temperature required. The simplest method is to use the temperature controller (see Fig. 1) to operate an electromechanical on/off contactor. When the furnace temperature falls below the required minimum, the contactor closes and the power is full on. When the temperature is too high, the power is switched off. This system necessarily incorporates backlash to avoid oscillation of the contact breaker, therefore the temperature regulation is inherently poor.

An improvement of this system is achieved by using two-step control. Here the power is switched between two levels, instead of off and on. If the heat losses of the furnace are constant and known, it is possible to arrange the two power levels to give a much more stable temperature than can be achieved with the simple on/off method. Other systems which have three-step control are also used.

Proportional Control

Where the work loading on a furnace is likely to vary, or a close tolerance is required over a wide range of temperature settings, proportional control is used. In this system, switching is replaced by continuous control of the power input, which is varied so as to supply the exact power required to maintain a steady furnace temperature. There are three commonly used methods of varying the power (see Fig. 1):

(i) The motor-driven variable transformer.
(ii) The saturable reactor.
(iii) The thyristor control.

The motor-driven variable transformer is both expensive and bulky, especially where high powers are concerned. Thyristor control is economical and relatively compact, and it provides temperature stability limited only by the performance of the temperature controller.

LOAD CHARACTERISTICS

In the design of a furnace control, the nature of the load must be taken into consideration. A number of different materials are used for the heating elements of electric furnaces, depending on the type of furnace and the temperature range to be covered. Some of these materials have a large positive temperature coefficient, so that the current taken from the supply when the furnace is switched on from cold may be several times the normal running current. Other materials have a minimum resistance at some intermediate temperature (Fig. 2).

Materials with a large temperature coefficient may require some current limiting to be included in the power control circuit so that the current taken during the heating-up period is not excessive. The design of current limit circuits is discussed in Ref. 1; a practical circuit is included in the present article.

PHASE CONTROL SYSTEMS

Proportional control of furnace power from the a.c. mains is readily achieved by phase control systems, which make use of the principle that a synchronous switch conducts for some chosen portion of the mains cycle. The larger this conducting portion is, the larger the power delivered to the load will be.

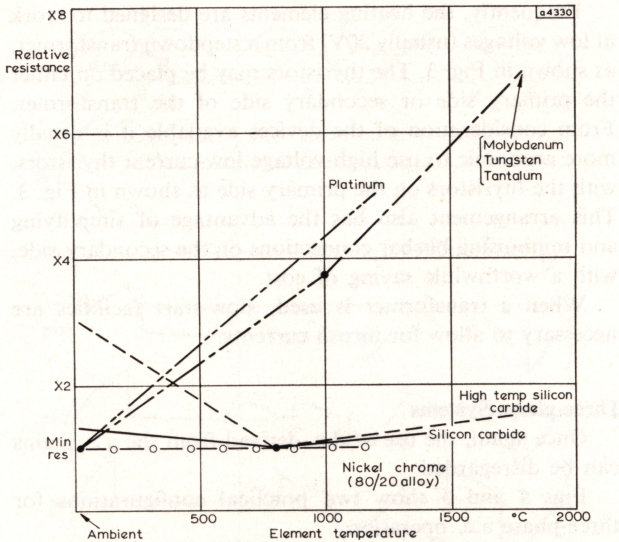


Fig. 2—Relative resistances of furnace element materials throughout their working temperature range
Note: Relative resistances are shown at ambient (switch-on) temperature, at the minimum-resistance point (for those materials that do not have minimum resistance at ambient), and at the maximum working temperature of the material. Relative resistances at other temperatures cannot necessarily be read off; nor can comparisons be made of the actual resistances of the different materials

Thyristors are ideal synchronous switches for furnace control, since they are able to control large powers at high efficiency. The thyristors are fired at the required point in the mains cycle by pulses that are supplied from a trigger module. The trigger module, in turn, is actuated by the 0 to 5mA output from the temperature controller.

Single-phase Systems

The heating elements can be supplied with d.c. derived from the a.c. mains by a bridge rectifier. However, d.c. supplies are not, in general, considered to be good practice because of the static fields developed both inside and outside the furnace.

Fig. 3 shows two alternative arrangements for controlling the a.c. power in a resistive load, each of which may be used with or without transformer output. The arrangement shown in Fig. 3b has the advantage that it protects the thyristors against reverse transients, at the cost of two rectifier diodes. However, the use of avalanche thyristors obviates the need for this circuit.

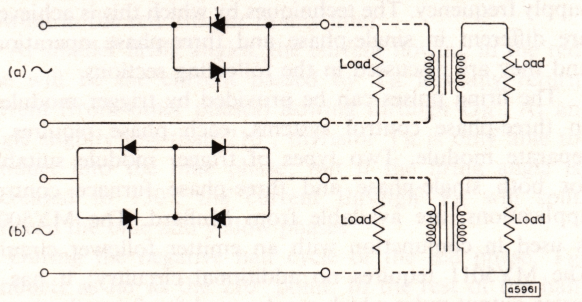


Fig. 3—Single-phase power controllers, with resistive or transformer-coupled load. The lower circuit is preferred

Frequently, the heating elements are designed to work at low voltages (usually 20V) from a stepdown transformer, as shown in Fig. 3. The thyristors may be placed on either the primary side or secondary side of the transformer. From consideration of the devices available it is usually more economic to use high-voltage low-current thyristors, with the thyristors on the primary side as shown in Fig. 3. This arrangement also has the advantage of simplifying and minimising busbar connections on the secondary side, with a worthwhile saving of cost.

When a transformer is used, slow-start facilities are necessary to allow for inrush currents.

Three-phase Systems

Once again, the use of d.c. derived from the a.c. mains can be disregarded.

Figs 4 and 5 show two practical configurations for three-phase a.c. operation.

The Fig. 4 circuit is rarely used for furnace control because the triggering circuitry is rather complex; but it has advantages if the harmonic content of the output waveform is of importance.

The Fig. 5 circuit is preferred. Three possible arrangements of load are shown. Connection of the thyristors on the primary side of the transformer is preferred, for the reasons already given. Again, slow start facilities are necessary to limit the inrush currents when a transformer is used.

It is also important, when using thyristors with transformers in furnace control systems, to ensure that the firing angles of the thyristors are balanced. This is to prevent the build-up of magnetic flux in the core due to the d.c. component. The circuits shown in Figs. 15 and 19, using the MY5001 and MY5011 thyristor trigger modules, can be balanced to better than 3° over the full control range. This has been found to be sufficiently accurate for most transformers. It is advisable, however, to tell the transformer manufacturer that the transformer is intended for use in a thyristor control system. He will then ensure that it is designed to operate at a lower maximum flux density. This will enable the transformer to tolerate slight unbalance between the phases.

THYRISTOR FIRING

In either single-phase or three-phase operation (Figs. 3, 4, or 5) the power supplied to the load is controlled by variation of the firing angle of the thyristors. In each case it is essential that the firing pulses are synchronised to the supply frequency. The techniques by which this is achieved are different in single-phase and three-phase operation, and they are discussed in the following sections.

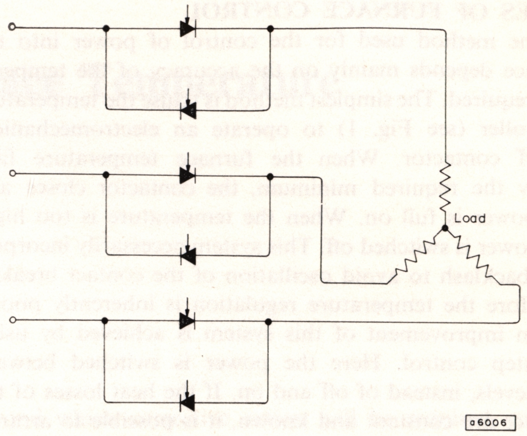


Fig. 4—Three-phase power controller

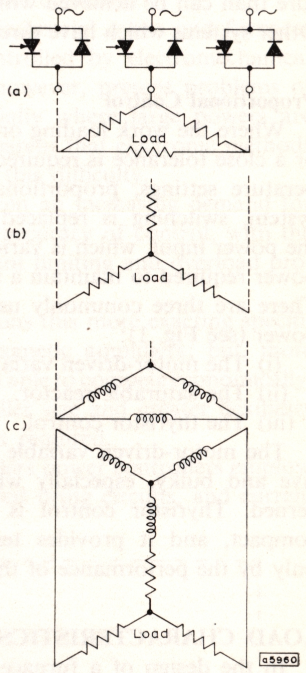


Fig. 5—Preferred circuit for three-phase power controller

(a) delta load
(b) star load
(c) transformer-coupled load

The firing pulses can be provided by trigger modules. In three-phase control systems, each phase requires a separate module. Two types of trigger module suitable for both single-phase and three-phase furnace control applications, are available from Mullard. The MY5001 is used in conjunction with an emitter follower circuit. The MY5011 requires no additional circuitry; it has a faster output pulse which can be used for firing thyristors in series or parallel; its longer pulse duration allows a more inductive load to be used; and it is more stable over a greater range of ambient temperatures.

Single-Phase Operation

In single-phase applications, synchronising of the MY5001 or MY5011 trigger module is achieved each time the a.c. supply voltage goes through zero. The output pulses will be timed from this point, and will appear every half cycle.

The relationship of firing angle and power output in a single-phase thyristor circuit is shown in Fig. 6. If the thyristor is fired at 0° (the start of the half cycle) then full power is delivered. The power is progressively reduced to zero as the firing angle is advanced from 0° to 180°. It should be noted that the conduction angle is the remaining part of the half cycle; so that:

firing angle + conduction angle = 180°.

The relationship between the power supplied to the load at a given firing angle θ, and the maximum possible power, is

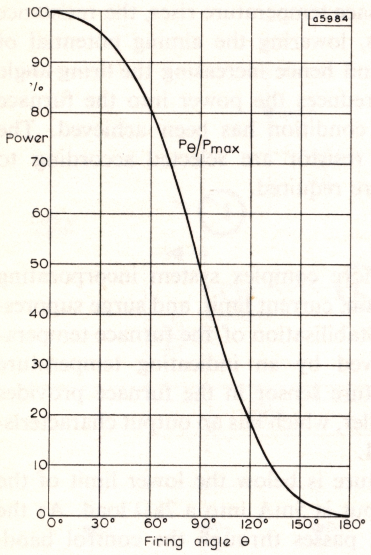


Fig. 6—Relationship between firing angle and power into a resistive load, for a single-phase a.c. controller

$$P_\theta/P_{max} = 1 - \left[\frac{1}{\pi}\left(\theta - \frac{\sin 2\theta}{2}\right)\right]$$

as plotted in Fig. 6.

Three-phase Operation

In three-phase a.c. controllers the range of firing required for full power control is 210°, therefore the simple type of synchronisation used in single-phase systems does not apply.

Little information is published on the waveforms obtained from a three-phase a.c. controller; and since this system is universally used in three-phase furnace control, it is worth spending some time on the explanation of the waveforms obtained.

The circuit diagram in Fig. 7 shows a three-phase a.c. controller with thyristors T_R, T_B, and T_Y in the red, blue, and yellow phases respectively. The related waveforms are shown in Fig. 8. The circuit operates in the following manner.

Consider the positive half cycle of the red phase. When the red thyristor T_R has been fired into conduction, current flows through the thyristor into the load and returns to the supply through one or both of the other phases. Thus, the return current flows through diode D_B, D_Y, or both. It will flow only into a phase that, at any particular moment, is more negative than the red phase; and, if both the blue and yellow phases are more negative than the red phase, then the return current will be shared between them in accordance with the potentials of the blue and yellow phases. Conduction ceases in the red phase only when there is no other phase at a more negative potential; that is, at 210°.

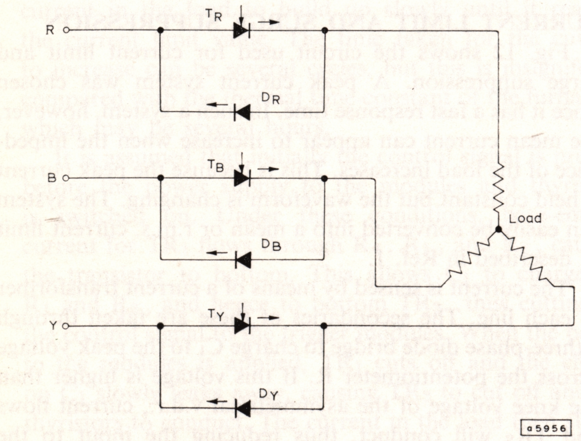


Fig. 7—Three-phase a.c. controller with star load

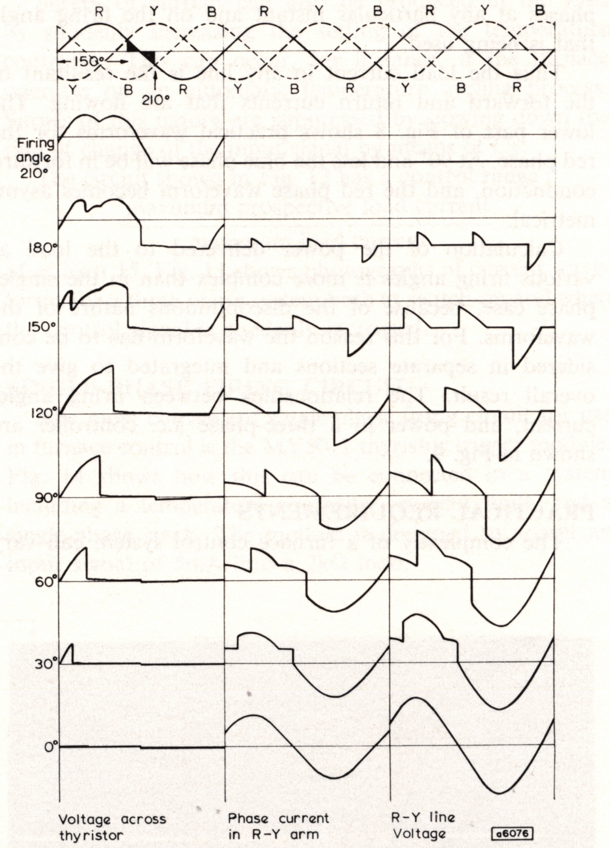


Fig. 8—Waveforms in three-phase a.c. controller

The lower part of Fig. 8 shows the voltage and current waveforms of the red phase. The 0° curves are obtained when the three thyristors are being fired at 0° (that is, at the starts of their positive half cycles). The other curves are for firing angles up to 210°.

If the firing angle of the thyristors is 210° (see the upper part of Fig. 8), then no current flows in the red thyristor, as already explained; there is no return current flowing through D_R from the yellow phase, because T_Y has not been fired; and the blue phase is at the same negative potential as the red phase. There is therefore no current flowing in the red line (or in any line).

At smaller firing angles, the current flowing in the red line will be the current passed by T_R less any return current (from other phases) flowing through D_R. At an angle slightly less than 210°, thyristor T_R is only able to conduct into the blue phase; but if the firing angle is decreased to 150°, the current through T_R will split between the blue and yellow phases.

During the negative half cycle of the red phase, T_R conducts as far as the 210° point. In the rest of the half cycle D_R may be carrying return current from one or both of the other phases, dependent on the potentials in those phases at any particular instant and on the firing angle that is being used.

Thus the load current in any line is the resultant of the forward and return currents that are flowing. The lower part of Fig. 8 shows practical waveforms for the red phase. At 90° and less the blue phase will be in forward conduction, and the red phase waveform becomes asymmetrical.

Calculation of the power delivered to the load at various firing angles is more complex than in the single-phase case, because of the discontinuous nature of the waveforms. For this reason the waveform has to be considered in separate sections and integrated to give the overall result. The relationships between firing angle, current, and power in a three-phase a.c. controller are shown in Fig. 9.

PRACTICAL REQUIREMENTS

The complexity of a furnace control system can vary considerably, depending on the accuracy required and the range of work the furnace has to deal with.

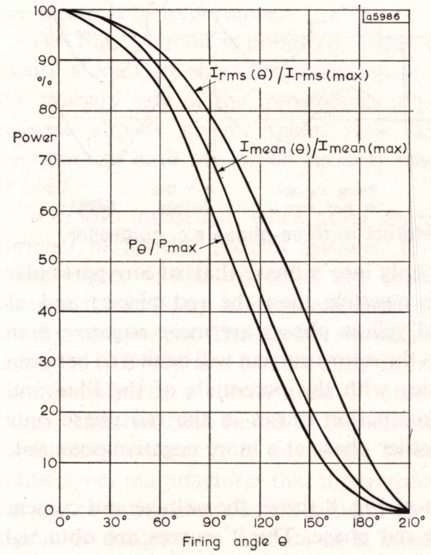


Fig. 9—Relationship between firing angle, current, and power, for a three-phase a.c. controller

Simple System

A simple open-loop single-phase control system may be constructed with the MY5001 trigger module and a single-phase stack. Typical stacks are the OTH10-608L d.c. stack and the OTH17-604 a.c. controller. The power delivered to the furnace is manually set by the resistor R (Fig. 10) which varies the firing angle of the thyristor in the stack.

The furnace temperature can be sensed by an n.t.c. thermistor (Fig. 10), and a simple feedback system stabilises the temperature. The thermistor and its series resistor are connected across the timing capacitor of the MY5001. When the thermistor is cold its resistance is high, and it has very little effect on the charging rate of the timing capacitor. As the furnace temperature rises, the resistance of the thermistor falls, lowering the aiming potential of the timing capacitor and hence increasing the firing angle of the thyristor. This reduces the power into the furnace until an equilibrium condition has been achieved. The thermistor and series resistor are selected according to the furnace temperature required.

Complex System

In most cases a more complex system incorporating temperature stabilisation, current limit, and surge suppression will be required. Stabilisation of the furnace temperature is usually achieved by an indicating temperature controller. A temperature sensor in the furnace provides a signal for the controller, which has an output characteristic as shown in Fig. 11.

When the temperature is below the lower limit of the control band, the output is 5mA into a 2kΩ load. As the temperature rises and passes through the control band, the current falls linearly until it is zero at the upper limit of the control band. The control band is shown as ±5% of the required temperature, but it can be almost any required tolerance. The 0 to 5mA output signal is used to control the triggering module and thus the power supplied to the furnace by the power controller.

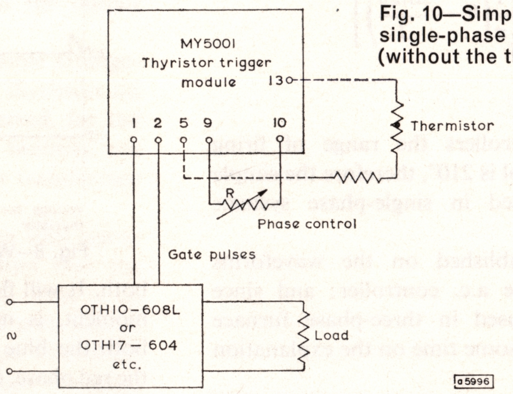


Fig. 10—Simple open-loop single-phase control system (without the thermistor)

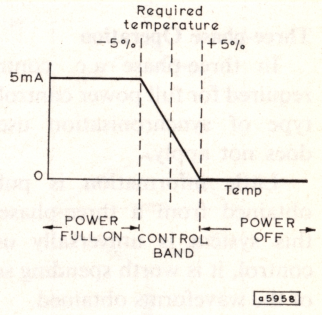


Fig. 11—Output signal from indicating temperature controller

CURRENT LIMIT AND SURGE SUPPRESSION

Fig. 12 shows the circuit used for current limit and surge suppression. A peak current system was chosen since it has a fast response time. In such a system, however, the mean current can appear to increase when the impedance of the load increases. This is because the peak current is held constant but the waveform is changing. The system can easily be converted into a mean or r.m.s. current limit as described in Ref. 1.

The current is sensed by means of a current transformer in each line. The secondaries of these are taken through a three-phase diode bridge to charge C_1 to the peak voltage across the potentiometer R. If this voltage is higher than the knee voltage of the asymmetrical v.d.r., current flows and TR_2 will conduct, thus reducing the input to the thyristor trigger module and the current in the load.

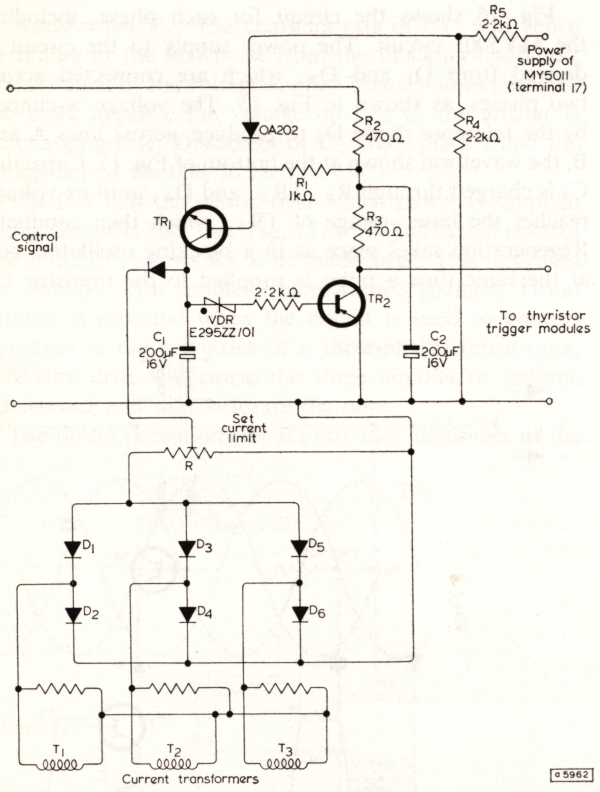


Fig. 12—Current limit and surge suppression circuit for furnace control system

The asymmetrical v.d.r. has a characteristic similar to that of a zener diode, but operates at a lower voltage. The v.d.r. used in this circuit has a knee voltage of only 1·3V, thus allowing the circuit to be used with current transformers having a lower VA rating than would be required if a zener diode were used.

Surge suppression is provided by TR_1. Without such a circuit, at the instant the supply to the thyristors (and hence to the load) was switched on, C_1 would be discharged, TR_2 would be cut off, and full power would be supplied to the load. This situation would continue until a sufficient potential had built up on C_1 to cause TR_2 to conduct and limit the current in the load.

The current limit circuit could be designed to operate after the first half cycle, but such circuits are prone to instability. A more satisfactory method is to allow the current in the load to build up slowly until it reaches the current limit value. The time taken for the current to increase can be several cycles, but this is insignificant compared with the thermal time-constant of the furnace—which may be several hours.

It is assumed that initially the control signal is present before the power supply to the modules and thyristors is switched on. Under these conditions, base-emitter current for TR_1 flows through R_4, R_1, and R_2, causing the transistor to bottom. This allows C_1 to charge via R_1 and R_2, and hence to bottom TR_2, thus cutting off the control signal to the trigger modules. When the power to the modules is applied, TR_1 cuts off and the charge on C_1 slowly leaks away, causing TR_2 to cut off and the thyristors to conduct. The current in the load then slowly builds up to the current limit level.

Surges of current can also be produced in the load by suddenly increasing the setting of the temperature controller. This can occur, for instance, if the furnace operates on an automatic temperature cycling process. Surges of this nature are suppressed by slowing down the rate of change of the input signal by means of C_2.

The circuit shown in Fig. 12 has a control range

$$\frac{\text{maximum prospective load current}}{\text{maximum load current}}$$

of at least 15. Fig. 13 shows photographs of current waveforms for a three-phase system both at switch-on and when the control signal is suddenly increased.

SINGLE-PHASE FIRING CIRCUIT

The most convenient single-phase firing circuit for use in furnace control is the MY5011 thyristor trigger module. Fig. 14 shows how this can be connected in a system including a temperature controller, current limit, and a single-phase stack. The module is designed to accept an input signal of 5mA into a 2kΩ load.

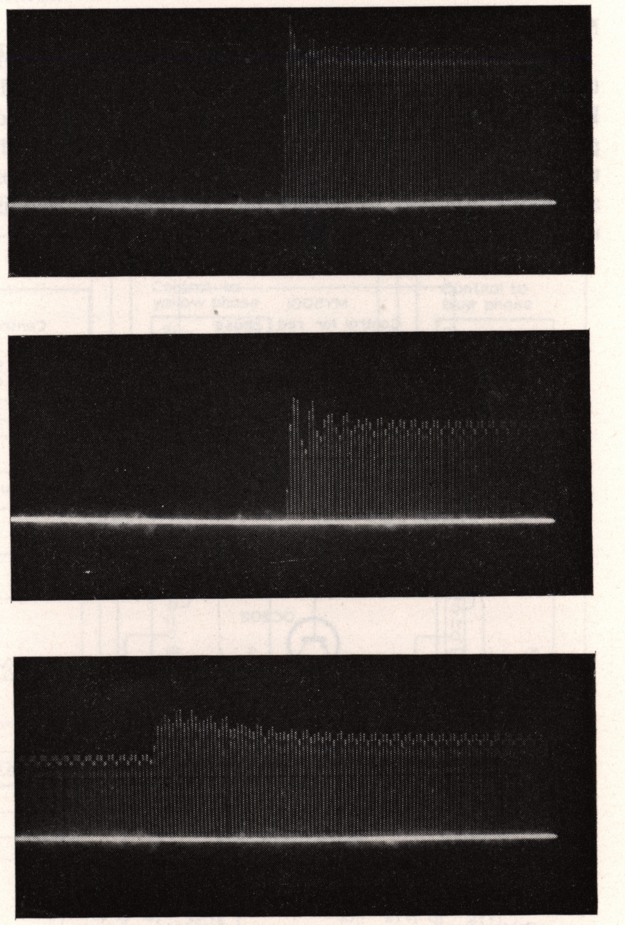


Fig. 13—Current limit waveforms

TOP: current in load at switch-on. Amplitude 3A, control ratio 10

CENTRE: current in load at switch-on. Amplitude 2A, control ratio 15

BOTTOM: Current in load when input control signal doubled. Amplitude 2A, control ratio 15

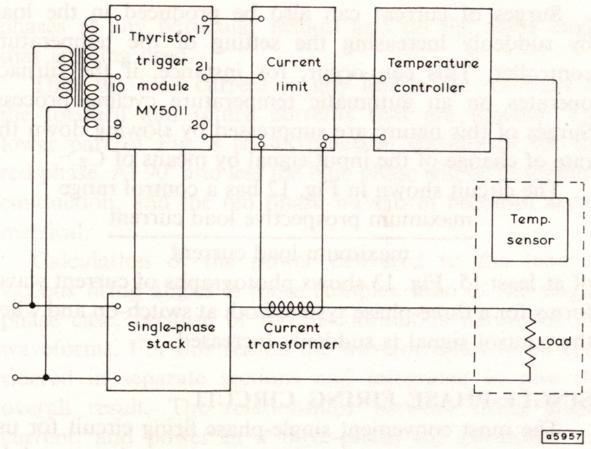

Thyristor trigger module MY5011
17
21
11
10
9
20
Current limit
Temperature controller
Temp. sensor
Single-phase stack
Current transformer
Load
a5957

Fig. 14—Single-phase furnace control system

THREE-PHASE FIRING CIRCUITS

As already explained, in three-phase systems each thyristor can conduct throughout the range 0 to 210°. Control of conduction angle in this range is provided by either the MY5001 or the MY5011.

MY5001 Circuit

Fig. 15 shows the method of using three MY5001 thyristor trigger modules in a three-phase furnace control. Each module is synchronised from two phases and provides control of the firing angle from 0 to 210°. With this module, extra circuitry is required. This consists of an emitter follower to replace the potentiometer that is usually used for the control of phase angle.

Fig. 16 shows the circuit for each phase, including the MY5001 circuit. The power supply to the circuit is derived from D_1 and D_2, which are connected across two phases, as shown in Fig. 15. The voltage is clipped by the reference diode D_3 to produce, across lines A and B, the waveform shown at the bottom of Fig. 17. Capacitor C_2 is charged through R_6, TR_2, and D_4, until its voltage reaches the base voltage of TR_1, which then conducts. Regeneration takes place as in a blocking oscillator, and at the same time a pulse is supplied to the thyristor via the transformer T_1. The charging rate of C_2, and hence the timing of the first pulse from the blocking oscillator, is determined by the voltage applied between lines C and B. The more negative the voltage on line C, the greater is the charging rate. Discharge of C_2 takes place when the voltage across D_3 falls to zero.

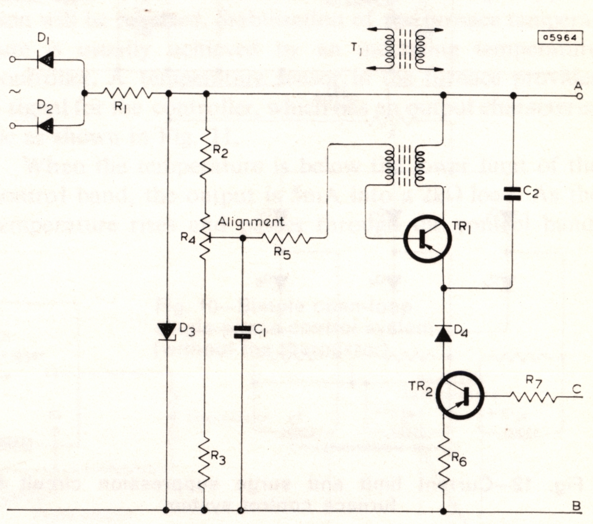

a5964
D_1
D_2
~
R_1
T_1
A
R_2
C_2
Alignment
R_4
R_5
TR_1
D_3
C_1
D_4
TR_2
R_7
C
R_3
R_6
B

Fig. 16—Operation of one phase of Fig. 15 circuit

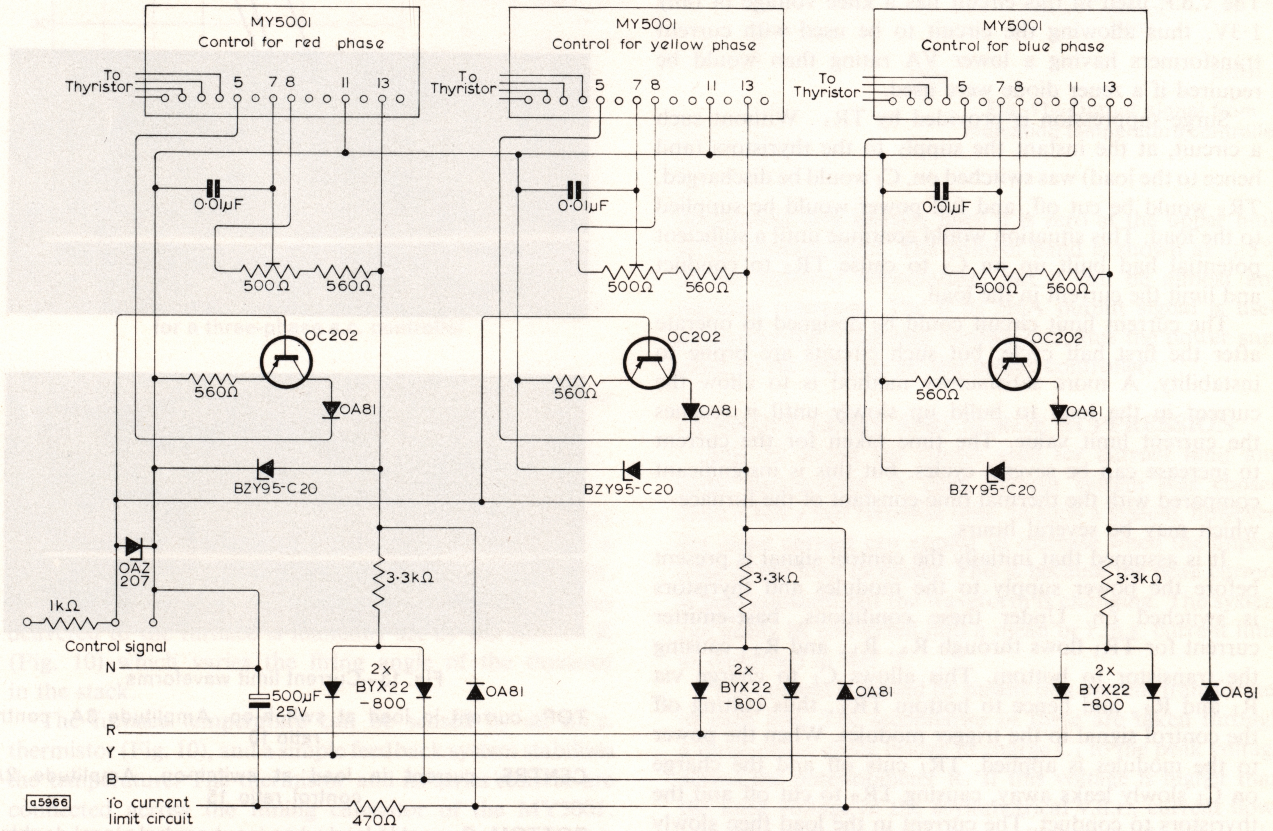

MY5001
Control for red phase
To Thyristor
5
7 8
11
13
MY5001
Control for yellow phase
To Thyristor
MY5001
Control for blue phase
To Thyristor
0·01μF
500Ω
560Ω
OC202
560Ω
OA81
BZY95-C20
OAZ 207
1kΩ
Control signal
N
R
Y
B
3·3kΩ
500μF 25V
2x BYX22 -800
OA81
470Ω
To current limit circuit
a5966

Fig. 15—Three-phase furnace control system using MY5001 trigger modules

The fact that the period over which power is supplied to this circuit is 300° (see Fig. 17) while the actual control period is 210°, allows R_6 to be made large. This improves the stability with ambient temperature changes. Good stability is essential when the circuit is used to control thyristors in the primaries of a three-phase transformer, since any drift will cause the three circuits to become unbalanced and may saturate the core.

The preset potentiometer R_4 provides alignment of the three phases, which can be made by means of lamp loads or, more accurately, by connecting all three units to the same two phases and observing the output voltage pulses from the modules on an oscilloscope.

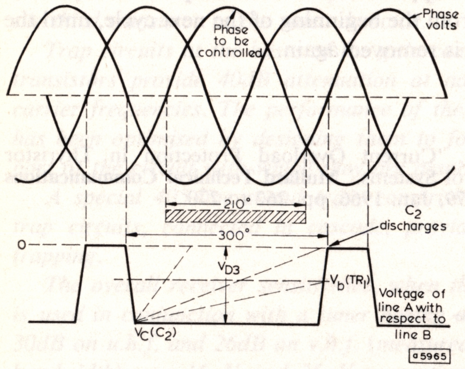


Fig. 17—Voltage waveforms in Fig. 16 circuit

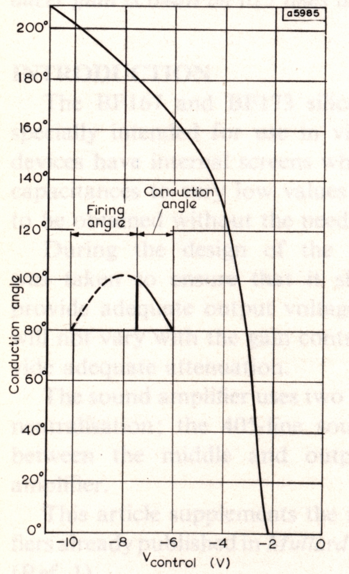


Fig. 18—Typical control characteristic of three-phase controller using MY5001 (Fig. 15 circuit)

The input control signal consists of a variable voltage 0 to 10V into 2kΩ. The *conduction* angle of the thyristor increases as the control voltage becomes more negative, as shown in Fig. 18.

The unit should preferably be connected to the supply through a star-star isolating transformer.

MY5011 Circuit

Three MY5011 trigger modules may be used in a three-phase system as shown in Fig. 19. When used with a three-phase a.c. controller each module must be operated from two phases through the balanced-secondary transformer MY5201.

The red phase is controlled by the positive half cycle of the voltage derived from the red and blue lines, and the negative half cycle of the voltage derived from the red and yellow lines. This allows 210° of firing angle control.

The potentiometer connected between terminals 14, 15, and 16 of each module ensures that all units are in

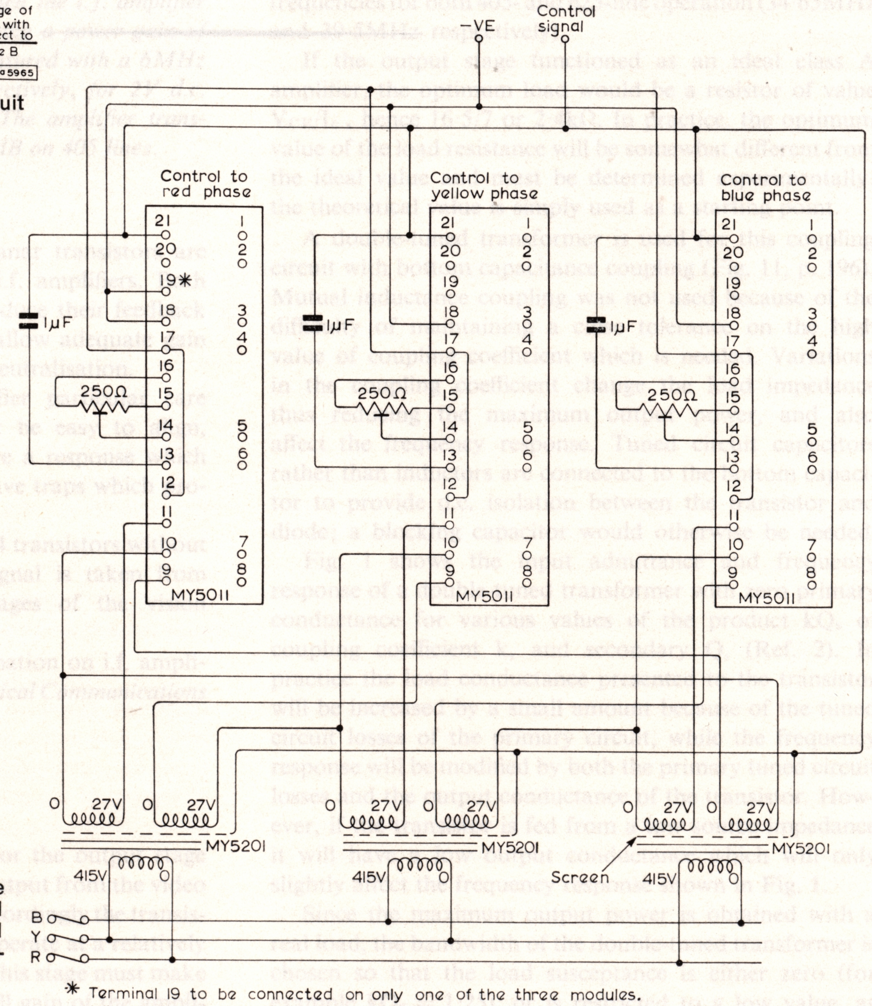

-VE
Control signal
Control to red phase
Control to yellow phase
Control to blue phase
21
20
19*
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
1μF
250Ω
MY5011
27V
MY5201
415V
Screen
B
Y
R

Fig. 19—Three-phase furnace control system using MY5011 trigger modules and MY5201 balanced-secondary transformers

* Terminal 19 to be connected on only one of the three modules. When current limit is used this connection should be removed to provide the required 2kΩ input impedance.

a5987

balance. The 1μF capacitor across terminals 13 and 21 increases the time-constant of the timing circuit to allow operation over the full 210° firing angle. The input signal from the temperature controller is 0 to 5mA into 2kΩ, giving a linear control of firing angle with voltage.

Balancing is best carried out by means of an oscilloscope. An ammeter in each line or (where the power control unit is an a.c. controller) lamp loads may also be used.

PERFORMANCE

The stability of furnace temperature that can be attained with the 'complex' systems is dependent on the capabilities of the indicating temperature controller and on the thermal design of the furnace.

COMPLETE CYCLE CONTROL

In phase control systems the power is controlled by chopping the sinusoidal mains voltage. The voltage across the load may therefore change from zero to several hundred volts in a few microseconds. This may be a serious source of interference to adjacent apparatus. If this interference is unacceptable it may be minimised by switching on complete cycles from the supply and ensuring that switching takes place only at the beginning of the cycle; that is, at low energy levels.

Such a system can only be an on/off one. If thyristors are used instead of an electromechanical contactor it is possible to reduce the difference between the on and the off temperatures, thus obtaining better temperature stability than with the conventional on/off system.

The circuits shown in Figs. 14 and 19 for the phase control of a furnace using the MY5011 may be used for such a system. The MY5011 has the inherent feature that any change in the input control signal during a cycle will not change the firing angle of the output until the beginning of the next cycle. Thus if a zero control voltage is applied to the module, the thyristors will be non-conducting; if −10V is applied at the control input, the thyristors will conduct from the beginning of the next cycle, until the control signal is removed again.

REFERENCE

1. Merrett, J. 'Current Overload Protection in Thyristor Phase Control Systems.' **Mullard Technical Communications** Vol. 8, No. 79, Jan. 1966, pp. 262 to 270.

I.F. Amplifier for Dual-standard Television Receivers

R. Bridgen, F. Grant, and W. Oxenford
Mullard Central Application Laboratory

Single-tuned circuits are used for coupling between the first, second, and third transistors of the vision i.f. amplifier, and a bottom capacitance coupled bandpass filter couples the third transistor to the video detector.

Trap circuits at the bases of the gain control and output transistors provide 40dB attenuation at adjacent channel carrier frequencies. The performance of these trap circuits has been optimised by designing them to form an integral part of the circuit with which they are associated.

A special 405-line sound trap, comprising two bridged trap circuits, connected in cascade, provides broad deep trapping.

The overall receiver sensitivities, when the i.f. amplifier is used in conjunction with a tuner having a power gain of 30dB on u.h.f. and 26dB on v.h.f. (measured with a 6MHz bandwidth), are 16μV and 35μV respectively, for 2V d.c. at the detector at the peak response. The amplifier transducer gain is 64dB on 625 lines and 62dB on 405 lines.

INTRODUCTION

The BF167 and BF173 silicon planar transistors are specially intended for use in vision i.f. amplifiers. Both devices have internal screens which reduce their feedback capacitances to very low values and allow adequate gain to be obtained without the need for neutralisation.

During the design of the amplifier particular care was taken to ensure that it should: be easy to align, provide adequate output voltage, have a response which will not vary with the gain control, have traps which provide adequate attenuation.

The sound amplifier uses two BF194 transistors without neutralisation; the 405-line sound signal is taken from between the middle and output stages of the vision amplifier.

This article supplements the information on i.f. amplifiers already published in *Mullard Technical Communications* (Ref. 1).

VISION AMPLIFIER

Output Stage

The most important requirement for the output stage is that it should provide an adequate output from the video detector with the required linearity. Accordingly the transistor used in this stage must be able to operate at a relatively high collector dissipation. In addition this stage must make a reasonable contribution to the overall gain of the amplifier.

The BF173 can be operated at a collector dissipation of 115mW at ambient temperatures up to 55°C, plus a 50% increase in dissipation due to supply voltage and resistor tolerances. A suitable d.c. operating point is $V_{CE} = 16{\cdot}5V$ and $I_c = 7mA$. For these d.c. conditions a switch-on surge which causes a 50% increase in supply voltage for 20 seconds can be tolerated without exceeding the voltage or dissipation ratings of the transistor.

The coupling circuit between the transistor and the video detector is designed so that the load impedance at the collector of the transistor is the optimum value for obtaining the maximum output power at the vision carrier frequencies for both 405- and 625-line operation (34·65MHz and 39·5MHz respectively).

If the output stage functioned as an ideal class A amplifier, the optimum load would be a resistor of value V_{CE}/I_c, hence 16·5/7 or 2·4kΩ. In practice, the optimum value of the load resistance will be somewhat different from the ideal value and must be determined experimentally; the theoretical value is simply used as a starting point.

A double-tuned transformer is used for this coupling circuit with bottom capacitance coupling (Fig. 11, p. 196). Mutual inductance coupling was not used because of the difficulty of maintaining a close tolerance on the high value of coupling coefficient which is needed. Variations in the coupling coefficient change the load impedance thus reducing the maximum output power, and also affect the frequency response. Tuned circuit capacitors rather than inductors are connected to the bottom capacitor to provide d.c. isolation between the transistor and diode; a blocking capacitor would otherwise be needed.

Fig. 1 shows the input admittance and frequency response of a double-tuned transformer with zero primary conductance for various values of the product kQ_s of coupling coefficient k, and secondary Q, (Ref. 2). In practice the load conductance presented to the transistor will be increased by a small amount because of the tuned circuit losses of the primary circuit, while the frequency response will be modified by both the primary tuned circuit losses and the output conductance of the transistor. However, if the transistor is fed from a low source impedance it will have a low output conductance which will only slightly affect the frequency response shown in Fig. 1.

Since the maximum output power is obtained with a real load, the bandwidth of the double-tuned transformer is chosen so that the load susceptance is either zero (for example $kQ_s = 1{\cdot}25$), or is restricted to a low value, as shown by the dashed line, for example.

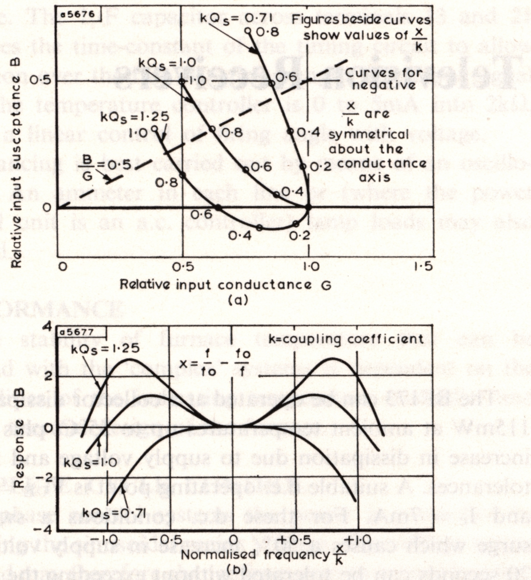


Fig. 1—Input admittance (a) and frequency response (b) of a double-tuned transformer with zero primary conductance

In Table 1 the values of the secondary Q, the coupling coefficient, and the total primary and secondary capacitances have been calculated for the above cases for a 2·4kΩ or 0·42mmho load conductance and for carrier frequencies of 34·65MHz and 39·5MHz. (The input conductance at centre frequency is given by: $k^2Q_sB_p$ where B_p is the susceptance of the total primary tuning capacitance C_p). The total secondary tuning capacitance C_s has been calculated for a typical conductance of 0·4mmho across the secondary.

TABLE 1

Calculated Design Values for the Output Transformer for Different Values of kQ_s

kQ_s	1·25		1·0	0·7
x/k	0·6	0·9	0·8	0·55
k	0·22	0·14	0·16	0·24
Q_s	5·7	9·0	6·2	3·0
C_s	10	15	10	5 pF
C_p	10	23	18	12 pF

where:

Q_s = secondary Q
x = $(f/f_o)-(f_o/f)$
k = coupling coefficient

Fig. 1 shows that $kQ_s = 1{\cdot}25$ causes considerable double humping of the response curve, while a very low secondary tuning capacitance is needed with $kQ_s = 0{\cdot}7$. It was therefore decided to use $kQ_s = 1$ and to fill in the dip in the response curve by using a single-tuned circuit between the middle and output stages. With Table 1 as a guide, the values of the secondary and bottom coupling capacitors were determined experimentally for the predicted frequency response, and of the primary capacitor for the maximum output. The maximum linear output was determined by measuring the d.c. output from the detector against the relative value of the i.f. input at carrier frequency; the results of these measurements are shown in Fig. 2.

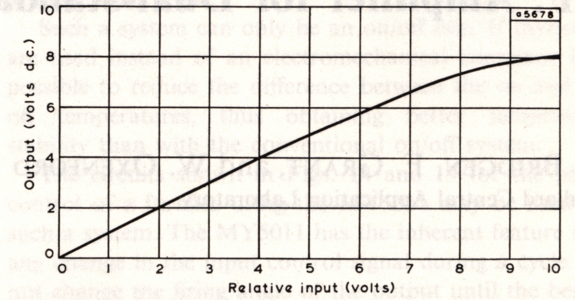


Fig. 2—Typical output linearity, 405-line and 625-line operation

Fig. 3 shows the measured sensitivity at the transistor bases for the complete amplifier, from which it is seen that 12mV is needed at the output transistor base for 2V d.c. output into the 3·9kΩ load. This corresponds to a power gain of 24dB for the combination of output transistor and video detector, if it is assumed that the input conductance of the stage is provided entirely by the 33Ω resistor (R_{17} in Fig. 11), which is included to provide good stability. The power gain of the output stage is thus 27dB for a typical power loss of 3dB in the video detector.

Middle Stage

The transistor TR_2 in the middle stage is coupled to the output transistor TR_3 by a single-tuned circuit (L_8, C_{18}), and by two trap circuits (L_{11}, C_{26}), (L_{12}, C_{27}), at the base of the output transistor (Fig. 11). The Q of the single-tuned circuit is chosen so that a flat-topped frequency response is obtained between the base of the middle transistor and the detector output. To avoid the need for readjustment of the output transformer after alignment of the interstage circuit, the interaction between these circuits, (L_8, C_{18}) and (L_{11}, C_{26}) (L_{12}, C_{27}), via the transistor must be kept small. This is achieved by the 33Ω resistor (R_{17} in Fig. 11) connected between the base and emitter of the output transistor, which minimises the effects of the collector-to-base feedback.

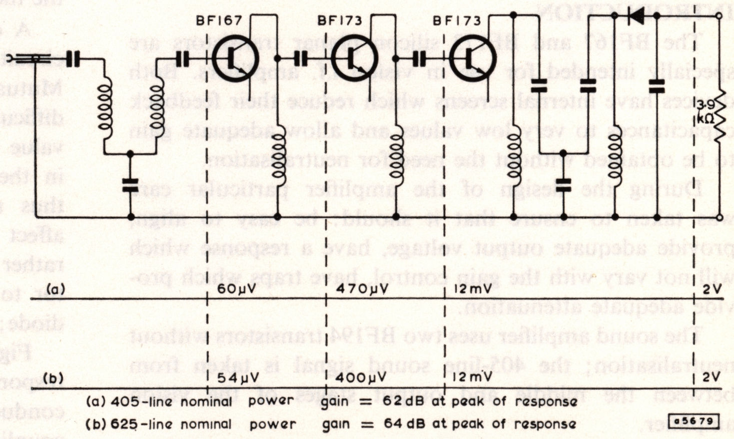

BF167
BF173
BF173
3·9 kΩ
(a)
60μV
470μV
12mV
2V
(b)
54μV
400μV
12mV
2V
(a) 405-line nominal power gain = 62 dB at peak of response
(b) 625-line nominal power gain = 64 dB at peak of response
a5679

Fig. 3—Signal levels in the amplifier and overall gain

As the 405-line sound signal is taken off between the middle and output stages, the signal handling performance of the middle stage must be sufficiently good to avoid sound-on-vision cross-modulation. The cross-modulation performance depends on the d.c. operating point, and it has been found that a suitable d.c. operating point for the BF173 is $V_{CE} = 10V$, $I_c = 7mA$.

To assess the cross-modulation performance of the middle stage by itself, the middle stage of the complete amplifier (Fig. 11) was converted into a test circuit (Fig. 4).

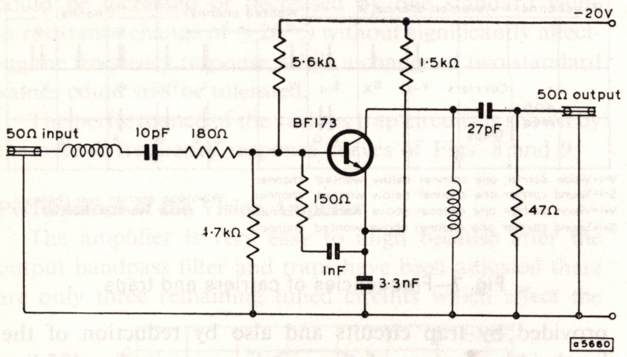


Fig. 4—Test circuit for measuring the cross-modulation of the middle stage

The interfering signal (38·15MHz) for 1% cross-modulation was then measured with a wanted signal (34·65MHz) at a level corresponding to 5V d.c. output from the detector. It was found that the interfering signal at the base, for 1% cross-modulation, was 5mV compared with a wanted signal of 1·2mV. Since the transmitted sound signal is nominally 6dB less than the vision signal, the nominal interfering signal at the base is 0·6mV, which is 18dB below the level for 1% cross-modulation. This margin is adequate to allow for a change in sound-to-vision ratio in the first stage of the amplifier and also for a possible change of ±10dB because of differences in propagation of the sound and vision carriers.

Gain Control Stage

The gain control transistor (TR_1) is operated on a 550Ω d.c. load line (R_5, R_6, R_{27} and R_{13} in Fig. 11) from an effective supply voltage of 14V. However, different d.c. load lines, which may be made necessary by consideration of the delayed a.g.c. circuit, may be used provided that care is taken that the maximum collector dissipation rating cannot be exceeded. The BF167 can be operated at 85mW at ambient temperatures up to 55°C plus a 40% increase in dissipation due to supply voltage and resistor tolerances. Operation at a lower dissipation is necessary when there are large switch-on surges.

The coupling circuit between the transistors in the gain control and middle stages is designed so that the large change in output conductance of the gain control transistor, which occurs when this transistor is gain controlled, has only a small effect on the overall frequency response. In this amplifier a single-tuned circuit has been used. At maximum gain this circuit has a Q of 3 and makes a slight contribution to the overall selectivity; as the gain is reduced the Q decreases and the contribution to the overall selectivity also decreases.

When a low-Q single-tuned circuit is used for interstage coupling there is some difficulty in presenting a sufficiently high load impedance to the first transistor. A low impedance causes low gain and reduces the gain control range of the first transistor since part of the gain reduction is caused by the increase in output conductance of this transistor.

A load impedance of approximately 1kΩ has been obtained by increasing the input resistance of the transistor in the middle stage by means of a resistor connected in series with the base (R_7 in Fig. 11). While improving the gain control range, this technique does not of course increase the gain. The resistor also increases the stability of the middle stage. However, an additional resistor (R_9) was added between the base and emitter of TR_2 to lower the output conductance of this transistor and hence the damping of the following tuned circuit; the stability was still further improved.

The coupling circuit at the amplifier input comprises: a circuit which simulates the tuned circuit in the tuner (L_1, C_1); the input tuned circuit of the i.f. amplifier (L_2, C_5); two shunt trap circuits; and a series-connected trap. The shunt trap circuits are effectively series-tuned circuits, one tuned above (41·5MHz) and the other tuned below (33·15MHz) the amplifier centre frequency. At a frequency between the two trapping frequencies the two traps form a parallel-resonant circuit, and by suitable choice of the relative L/C ratios this parallel resonance can be made to occur at the amplifier centre frequency.

The effect of the two shunt traps is thus to change the input transformer from a double-tuned circuit into a triple-tuned circuit. The bandwidth of this circuit can be adjusted by changing the L/C ratio of the tuned circuit at the amplifier input (L_2, C_5), while the degree of double humping can be controlled by the bottom coupling capacitor (C_2+C_3); the bandwidth of the circuit (L_1, C_1) simulating the tuned circuit of the tuner must be made approximately equal to the required overall bandwidth. The circuit up to the base of the BF167 was adjusted to give a flat-topped frequency response when disconnected from the base of the transistor. When the circuit was connected to the transistor, however, it was found necessary to add a 100pF capacitor (C_{12}) in series with the base to reduce the effect of a change of transistor input impedance with gain control.

For 405-line operation the frequency of the 41·5MHz trap is changed to 39·65MHz; the value of the bottom coupling capacitor is reduced by 39pF and a different input tuned circuit (L_3, C_6) is used. The separate input tuned circuits allow independent adjustments to be made to the frequency response for both 405- and 625-line operation. The frequency response of the complete input circuit for 625- and 405-line operation is shown in Figs. 5 and 6. The frequency response is practically unaffected by gain control.

The results of measurement of the gain control characteristic, cross-modulation performance, and gain are given in Table 2, page 195.

Adjacent Channel and Sound Traps

Fig. 7 shows the frequencies of the wanted and adjacent channel carriers and of the traps which have been used. All the adjacent channel traps (A, B, and C) are included in the input circuit, while the sound traps (D, E, and G)

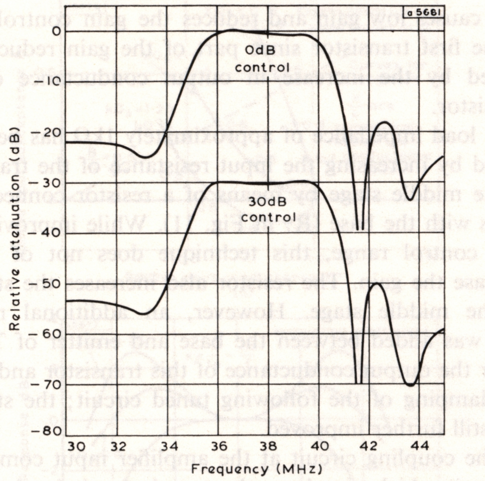


Fig. 5—Frequency response characteristics of the input circuit, 625-line operation

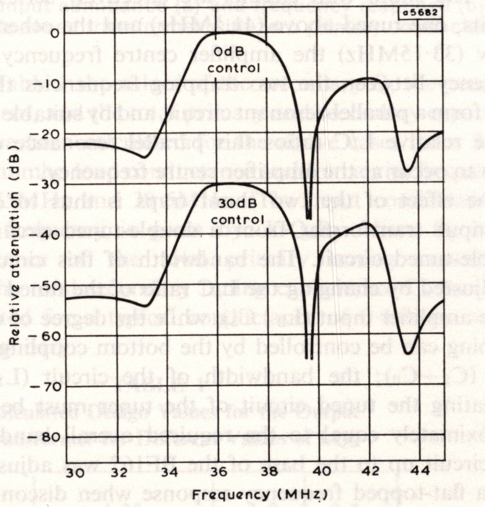


Fig. 6—Frequency response characteristics of the input circuit, 405-line operation

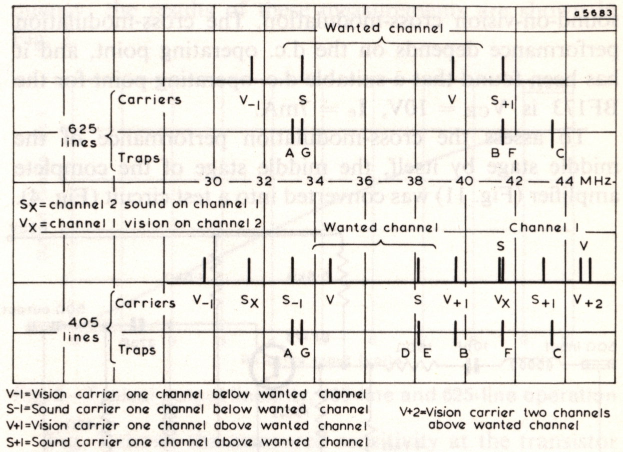

a5683
Wanted channel
625 lines
Carriers
Traps
V-1
S
V
S+1
A G
B F
C
30 32 34 36 38 40 42 44 MHz
Sx=channel 2 sound on channel 1
Vx=channel 1 vision on channel 2
Wanted channel
Channel 1
405 lines
Carriers
Traps
V-1
Sx
S-1
V
S
V+1
Vx
S+1
V+2
A G
D E
B
F
C
V-1=Vision carrier one channel below wanted channel
S-1=Sound carrier one channel below wanted channel
V+1=Vision carrier one channel above wanted channel
S+1=Sound carrier one channel above wanted channel
V+2=Vision carrier two channels above wanted channel

Fig. 7—Frequencies of carriers and traps

and a trap for channel 1 sound (F) are included between the middle and output stages. The 33·5MHz sound trap (G) and the 33·15MHz adjacent channel trap (A) are in circuit on both systems and thus assist each other; consequently low-Q traps are used which result in a very broad combined trap, and avoid trapping too deeply.

The design objective for the adjacent channel selectivity was that the response at an adjacent carrier frequency should be at least 40dB below the maximum response. It was fairly easy to meet this objective for the 625-line system because the frequencies of the adjacent channel carriers are well separated from the amplifier centre frequency. In addition the amplifier coupling circuits contribute to the overall selectivity.

On 405 lines, at frequencies between the amplifier centre frequency and 39·5MHz (the frequency of the vision carrier on the 625-line system), the amplifier coupling circuits make practically no contribution to the overall selectivity, because these circuits have been designed for the 625-line system. Consequently the selectivity, at frequencies from the sound carrier (38·15MHz) up to frequencies above the passband of the 625-line system, must be provided by trap circuits and also by reduction of the bandwidth of some of the coupling circuits for 405-line operation. In this amplifier the bandwidth of the input coupling circuit is changed as described in *Gain Control Stage*, (page 193). As trap B in the input circuit is less effective when tuned to a lower frequency (39·65MHz) for 405-line operation, a balanced bridge arrangement has been used to provide an effective increase in the Q of this trap.

The circuit of trap B is shown in Fig. 11. For 625-line operation inductor L_5 series-resonates with the parallel combination of capacitors C_8 and C_9; a perfect null is obtained when the value of resistor R_3 is four times the value of the equivalent series loss resistance of the tuned circuit by itself. For 405-line operation the trapping frequency is lowered by connecting a capacitor (C_4) across the inductor; this increases the optimum value for R_3 by a factor $[(C_4+C_8+C_9)/(C_8+C_9)]^2$. The value used for this resistor, therefore, must be a compromise.

The design objective for the 405-line sound trap was that the response at the sound carrier frequency should be 46dB below the maximum response, while a bandwidth of about 300kHz at 40dB attenuation was needed; the trap should also have as little effect as possible on the overall bandwidth of the vision amplifier. These objectives were achieved by using two bridged traps connected in cascade as shown in Fig. 11. The first trap D is essentially a parallel-tuned circuit connected in series with the signal, while the second trap F is essentially a series-tuned circuit connected across the signal path. The combination of these two traps provides adequate attenuation, and in addition behaves as a band stop filter, hence a good bandwidth is obtained.

Trap D comprises L_9 and C_{21} which parallel-resonates with the series combination of C_{22} and C_{23}. A perfect null is obtained when the value of resistor R_{12} is a quarter of the equivalent parallel loss resistance of the tuned circuit by itself. For this trap the impedance of the parallel-tuned circuit is reduced by using a capacitive tap. Trap E operates in a similar manner to trap B which has already been described.

The 405-line sound trap affects both the tuning and the losses of the coupling circuits between the middle and output stages. The change of tuning is counteracted by connecting a suitable value capacitor in place of the trap for 625-line operation, while the loss of gain is largely offset by disconnecting resistor R_{17}, for 405-line operation.

As the increase in effective Q of traps D and E (and B) depends on the balance of the bridge circuit, the effect of the tolerance of the balancing resistors R_{12} and R_{14} was investigated. It was found that the value of both resistors could be increased or decreased by one standard value (a resistance change of $\pm 20\%$) without significantly affecting the frequency response, while a change of two standard values could still be tolerated.

The performance of the various trap circuits is shown by the overall frequency response curves of Figs. 8 and 9.

Performance of the Vision Amplifier

The amplifier is very easy to align because after the output bandpass filter and traps have been adjusted there are only three remaining tuned circuits which affect the 625-line response. One of these (L_7, C_{15}) can be used to adjust the response at maximum gain, but it has virtually no effect at reduced gain. After the other two tuned circuits (L_8, C_{18} and L_2, C_5) have been adjusted for maximum gain the final response curve is obtained by a small simultaneous readjustment of these two tuned circuits.

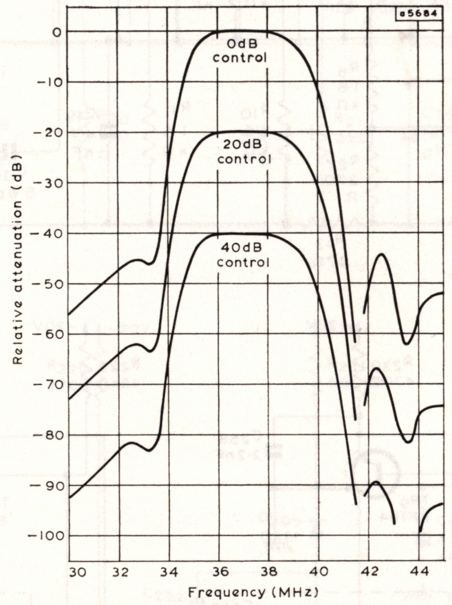


Fig. 8—Frequency response characteristics, 625-line operation

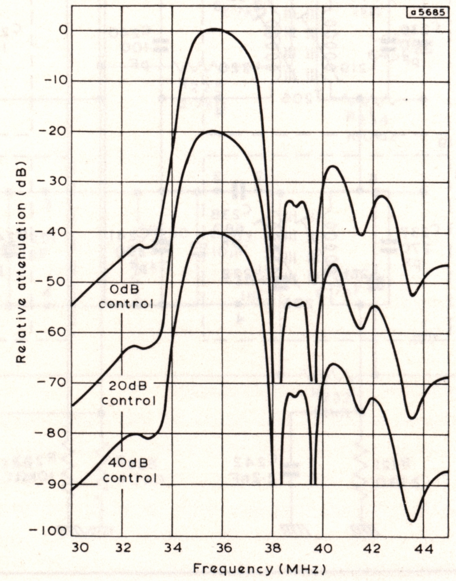


Fig. 9—Frequency response characteristics, 405-line operation

Three amplifiers have been constructed, and typical performance figures are given below:

Fig. 2	Typical output linearity 405- and 625-line operation
Fig. 3	Signal levels in the amplifier and overall gain
Fig. 8	Frequency response characteristics 625-line operation
Fig. 9	Frequency response characteristics 405-line operation
Fig. 10	Constant gain reduction.

The trap depths (Figs. 8 and 9) were measured by using a signal generator and d.c. meter, at a constant output level of 0·5V. It was also possible to measure the trap depths directly by using a Polyskop provided that the trace was expanded sufficiently to avoid the presence of overload signals.

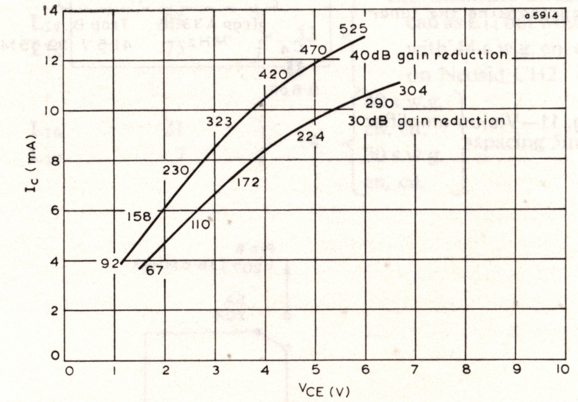


Fig. 10—Constant gain reduction. Figures beside the curves indicate the base current of the BF167 in microamperes

The overall sound-on-vision cross-modulation performance was measured by using two signal generators to represent the sound and vision carriers. The vision carrier generator was adjusted to maintain the output from the video detector at 5V d.c. at various values of gain reduction (Fig. 10), and the sound carrier generator was adjusted to give 1% sound-on-vision cross-modulation. The cross-modulation performance was then expressed as the Protection Ratio; that is the ratio of the sound carrier level required for 1% cross-modulation to the nominal sound carrier level. The results are given in Table 2.

TABLE 2

Protection Ratio

Overall sound-on-vision cross-modulation performance

Gain reduction dB	0	10	20	30	40
Protection ratio dB for 5V video output	13	14	15	20	10

The overall receiver sensitivities, when the i.f. amplifier is used in conjunction with a tuner having a power gain of 30dB on u.h.f. and 26dB on v.h.f. (measured with a 6MHz bandwidth), are 16μV and 35μV respectively, for 2V d.c. at the detector at the peak response. The amplifier transducer gain is 64dB on 625 lines and 62dB on 405 lines.

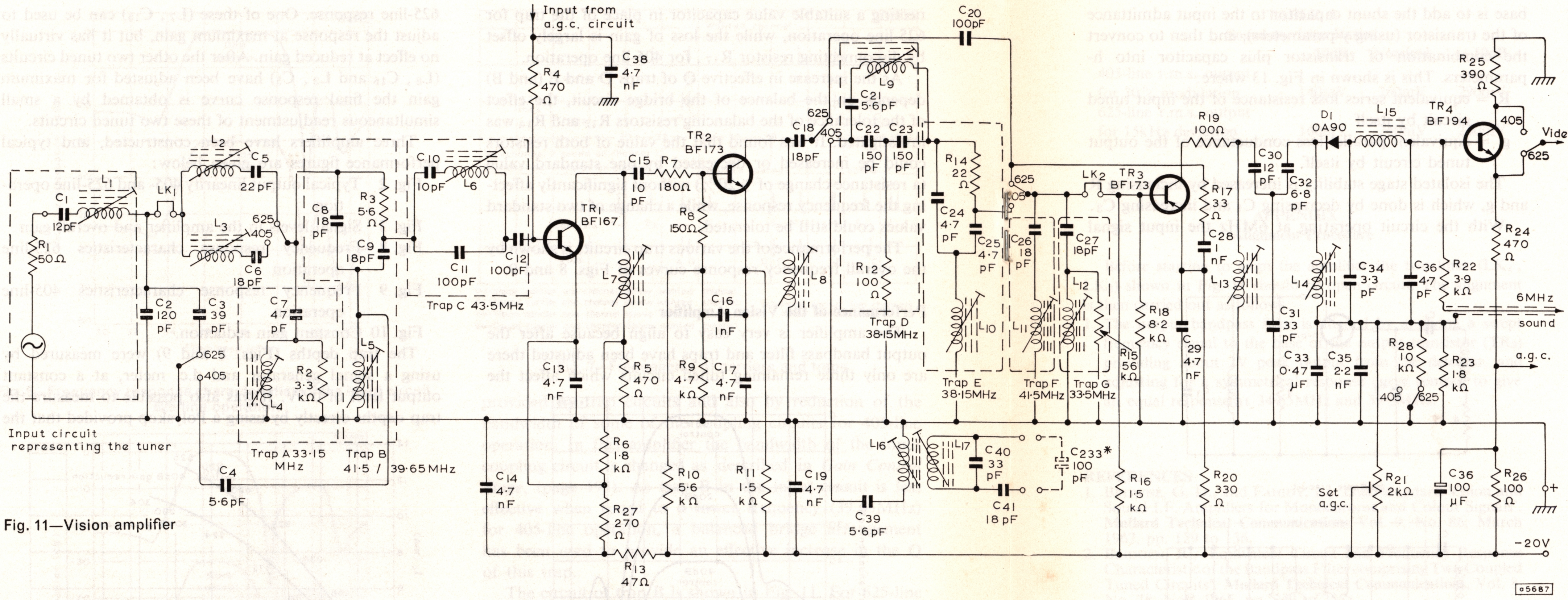

Input circuit representing the tuner
R1 50Ω
C1 12pF
L1
LK1
L2
C5 22pF
L3
C6 18pF
C2 120 pF
C3 39 pF
625
405
C7 47 pF
R2 3·3 kΩ
R3 5·6 kΩ
C8 18 pF
C9 18pF
L4
L5
Trap A 33·15 MHz
Trap B 41·5 / 39·65 MHz
C4 5·6pF
C10 10pF
L6
C11 100pF
C12 100pF
Trap C 43·5MHz
Input from a.g.c. circuit
R4 470
C38 4·7 nF
TR1 BF167
L7
C13 4·7 nF
R5 470 Ω
R6 1·8 kΩ
C14 4·7 nF
R27 270 Ω
R13 47Ω
C15 10 pF
R7 180Ω
R8 150Ω
TR2 BF173
L8
C16 1nF
R9 4·7 kΩ
C17 4·7 nF
R10 5·6 kΩ
R11 1·5 kΩ
C19 4·7 nF
C39 5·6pF
C18 18pF
L9
C21 5·6pF
C22 150 pF
C23 150 pF
R12 100 Ω
Trap D 38·15MHz
C20 100pF
R14 22 Ω
C24 4·7 pF
C25 4·7 pF
L10
Trap E 38·15MHz
L16
L17
C40 33 pF
C41 18 pF
C233* 100 pF
C26 18 pF
C27 18pF
L11
L12
Trap F 41·5MHz
Trap G 33·5MHz
LK2
TR3 BF173
R15 56 kΩ
R16 1·5 kΩ
R17 33 Ω
C28 1 nF
L13
R18 8·2 kΩ
C29 4·7 nF
R19 100Ω
C30 12 pF
C32 6·8 pF
C31 33 pF
C33 0·47 μF
C35 2·2 nF
R20 330 Ω
D1 OA90
L15
L14
C34 3·3 pF
TR4 BF194
C36 4·7 pF
R22 3·9 kΩ
R28 10 kΩ
R21 2kΩ
Set a.g.c.
C36 100 μF
R23 1·8 kΩ
R24 470 Ω
R25 390 Ω
R26 100 Ω
Video
6MHz sound
a.g.c.
-20V
a5687

Fig. 11—Vision amplifier

Coil Data for Vision Amplifier

All coils, except L_{15}, are wound on 5mm dia. formers, using Neosid 4×0·5×6mm screw cores. Coils L_1 to L_{14} are wound with 38 s.w.g. t.n.a. wire.

Winding	No. of turns	Former length (mm)	Comment
L_1	19	14	used only for measurements
L_2	12	14	wound on same former
L_3	15		
L_4	7	14	
L_5	7	14	
L_6	19	14	
L_7	19	14	
L_8	15	14	
L_9	33	14	
L_{10}	24	14	
L_{11}	12½	14	
L_{12}	16½	14	
L_{13}	18	14	
L_{14}	25	33	L_{15} mounted in same can as L_{14} but wound with 44 s.w.g. en. cu. on Neosid CH2.
L_{15}	75		
L_{16}	21	14	40 s.w.g. en. cu. 30 s.w.g. en. cu. spacing 5mm
L_{17}	7		

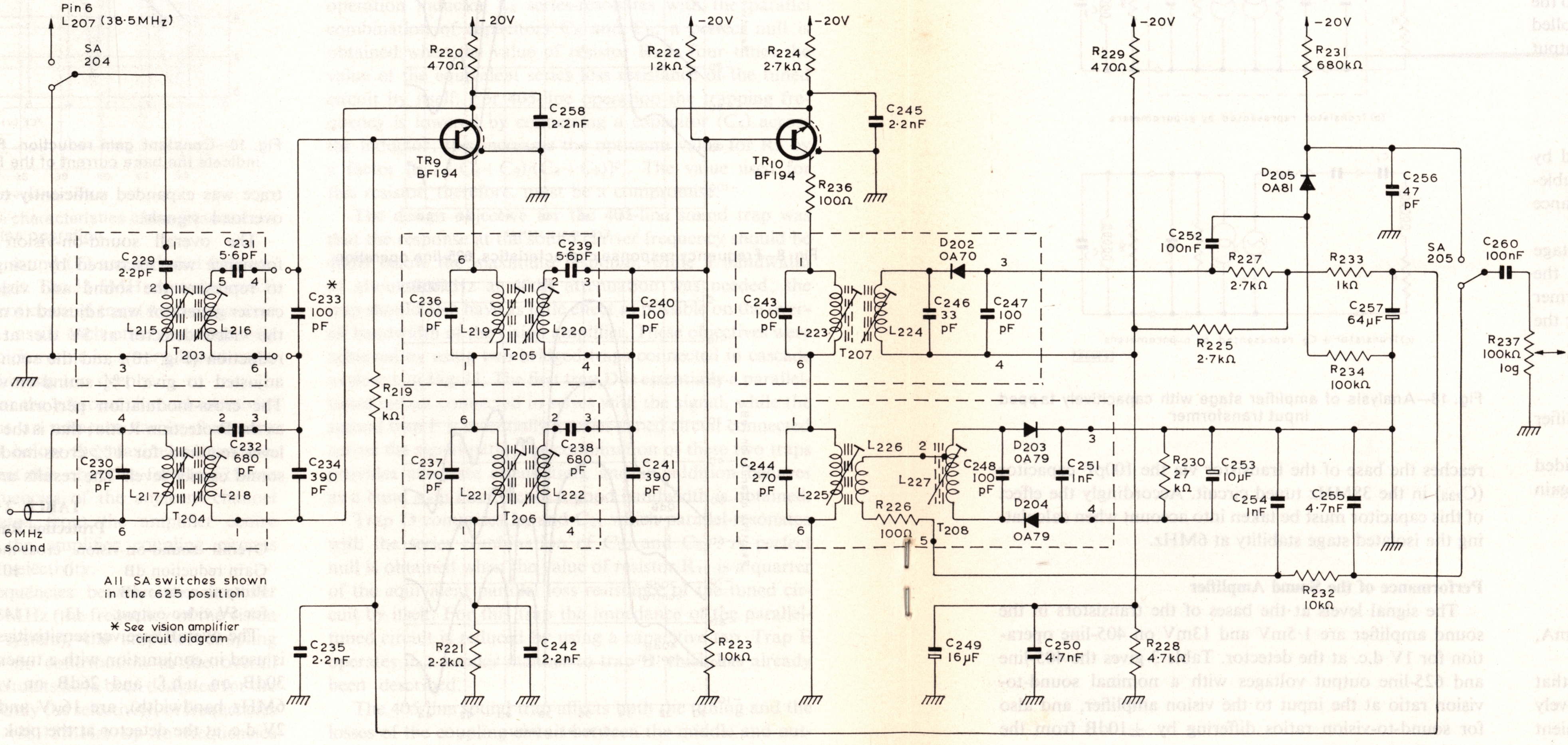

Pin 6 L207 (38·5MHz)
SA 204
6MHz sound
All SA switches shown in the 625 position
* See vision amplifier circuit diagram
-20V
R220 470Ω
C258 2·2nF
TR9 BF194
R222 12kΩ
R224 2·7kΩ
C245 2·2nF
TR10 BF194
R236 100Ω
C229 2·2pF
C231 5·6pF
L215
L216
T203
C233* 100 pF
R219 1 kΩ
C236 100 pF
L219
C239 5·6pF
L220
T205
C240 100 pF
C230 270 pF
C232 680 pF
L217
L218
T204
C234 390 pF
C237 270 pF
L221
C238 680 pF
L222
T206
C241 390 pF
C235 2·2nF
R221 2·2kΩ
C242 2·2nF
R223 10kΩ
C243 100 pF
L223
D202 OA70
C246 33 pF
C247 100 pF
L224
T207
C244 270 pF
L225
L226
L227
R226 100Ω
D203 OA79
D204 OA79
C248 100 pF
T208
C251 1nF
R230 27 kΩ
C253 10μF
C254 1nF
C255 4·7nF
C249 16μF
C250 4·7nF
R228 4·7kΩ
R229 470Ω
R231 680kΩ
D205 OA81
C256 47 pF
C252 100nF
R227 2·7kΩ
R225 2·7kΩ
R233 1kΩ
C257 64μF
R234 100kΩ
R232 10kΩ
SA 205
C260 100nF
R237 100kΩ log
Audio amplifier
a5695a

Fig. 12—6MHz/38MHz sound amplifier

*Connection to sound amplifier may be made by replacing T_{203} assembly and SA_{204} in the sound amplifier with connection to C_{233} as shown. An alternative vision i.f. amplifier, connected to this sound amplifier, is shown in Fig. 1 of Ref. 1.

SOUND AMPLIFIER

The sound amplifier (Fig. 12) is fairly conventional and has been described in a previous article (Ref. 1). The two BF194 transistors are operated at a nominal d.c. operating point of $V_{CE} = 10V$, $I_c = 3{\cdot}5mA$; the BF194 in the input stage is reverse gain controlled on 405-line operation.

Coupling Circuits and System Switching

Double-tuned transformers are used for all the coupling circuits; separate transformers are used for 6MHz and 38MHz, and the primaries and secondaries of each pair of transformers are connected in series.

The only system switches are the vision amplifier switch, which connects the 38MHz signal for 405-line operation, and the audio output switch.

A.G.C. Circuit

The a.g.c. control voltage is derived directly from the a.m. detector and is applied in series with the bias supply to the base of the first transistor. When there is no 38MHz sound carrier (625-line operation) the first transistor is biased to its nominal operating point. The effects of spreads in the base current of this transistor have been minimised by keeping the resistance of the a.g.c. circuit in series with the base as small as possible. A larger value of emitter resistor cannot be used with this transistor as this would require a larger bias voltage which in turn would lead to the output voltage from the a.m. detector being controlled at a higher value. With the present circuit the d.c. output voltage is controlled at 1·7V.

Stability

Stable operation of the amplifier stages is ensured by capacitively tapping the secondaries of the double-tuned circuits and by using adequately low-impedance primary circuits.

The isolated stability factor (η_i) of an amplifier stage comprising the secondary of the input transformer, the transistor, and the primary of the output transformer can be calculated by using the following definition for the stability factor (Refs. 3 and 4).

$$\eta_i = \frac{2R_e(P_{11})R_e(P_{22}) - R_e(P_{12}P_{21})}{|P_{12}P_{21}|},$$

where P represents the two port parameters of the amplifier stage expressed in y-, z-, or h-parameters.

It can be shown that instability cannot occur provided η_i is greater than unity, and that the maximum power gain is given by:

$$G_{max} = \frac{1}{S_i}\left|\frac{P_{21}}{P_{12}}\right|$$

where

$$S_i = \eta_1 + (\eta_1^2 - 1)^{\frac{1}{2}}.$$

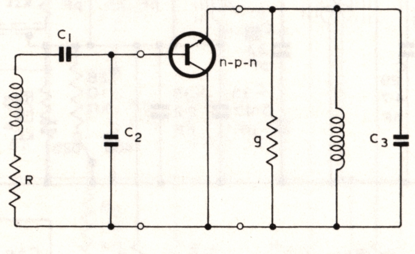
For the BF194 at 38MHz, operated at 10V, 3·5mA, and for $S_i = 2$, the maximum power gain is 23dB.

With the circuit operating at 38MHz it is found that the 6MHz circuits at the base and collector have relatively low impedances and can be neglected. A convenient method of handling the capacitor divider circuit at the base is to add the shunt capacitor to the input admittance of the transistor (using y-parameters), and then to convert the combination of transistor plus capacitor into h-parameters. This is shown in Fig. 13 where:

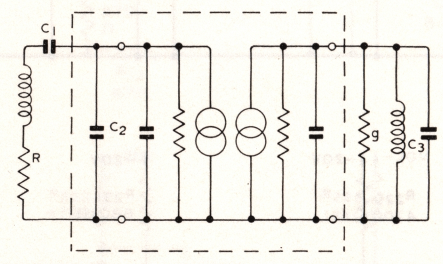
R = equivalent series loss resistance of the input tuned circuit by itself

g = equivalent parallel loss conductance of the output tuned circuit by itself.

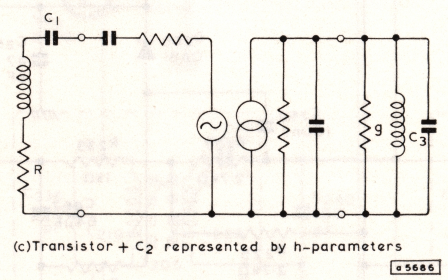
The isolated stage stability is increased by increasing R and g, which is done by decreasing C_1 and increasing C_3.



(a) Basic circuit



(b) Transistor represented by y-parameters



(c) Transistor + C2 represented by h-parameters

Fig. 13—Analysis of amplifier stage with capacitively tapped input transformer

With the circuit operating at 6MHz the input signal reaches the base of the transistor via the 100pF capacitor (C_{233}) in the 38MHz tuned circuit. Accordingly the effect of this capacitor must be taken into account when calculating the isolated stage stability at 6MHz.

Performance of the Sound Amplifier

The signal levels at the bases of the transistors in the sound amplifier are 1·5mV and 13mV on 405-line operation for 1V d.c. at the detector. Table 3 gives the 405-line and 625-line output voltages with a nominal sound-to-vision ratio at the input to the vision amplifier, and also for sound-to-vision ratios differing by ±10dB from the nominal.

TABLE 3
Sound-to-vision Ratios

	−10dB	Nominal	+10dB
405-line r.m.s. output for 30% modulation	140mV	260mV	290mV
625-line r.m.s. output for 15kHz deviation	160mV	240mV	250mV

APPENDIX 1
Alignment Procedure

Before starting to align the amplifier the two links (LK_1, LK_2) shown in Fig. 11 should be open circuit. The alignment is then carried out as follows:

1. The output bandpass filter is aligned by applying a swept frequency signal to the base of the output transistor (TR_3) providing about 2V peak output from the detector, and adjusting for a symmetrical response curve centred to give an equal response at 34·65MHz and 39·5MHz.
2. The tuner i.f. tuned circuit is peaked to 37·3MHz.
3. The two links (LK_1, LK_2) are replaced and L_2, L_7, and L_8 are adjusted initially in the 625-line position for maximum output with 30dB gain control.
4. Traps A, C, F, and G are adjusted in the 625-line position and trap B in the 405-line position.
5. L_2 and L_8 are adjusted to final setting, by using a swept frequency signal in the 625-line position, to give a flat-topped response curve with the response 6dB down at 39·5MHz.
6. L_7 is adjusted to final setting at maximum gain to give a flat-topped response curve, and then 30dB gain control is again applied.
7. Traps D and E, comprising the 405-line sound trap, are adjusted to give maximum attenuation at 38·15MHz by using a swept frequency signal.
8. The 38·15MHz and 6MHz sound amplifiers must then be aligned.
9. Finally, L_3 is adjusted by using a swept frequency signal, in the 405-line position, so that the response is 6dB down at 34·65MHz.

REFERENCES

1. BROWNE, G. D., and FAHIDY, L., 'Dual-standard Vision and Sound I.F. Amplifiers for Monochrome and Colour Signals'. **Mullard Technical Communications** Vol. 9, No. 86, March 1967, pp. 129 to 136.
2. BRIDGEN, R., 'Equivalent Circuit and Frequency Response Characteristic of the Bandpass Filter comprising Two Coupled Tuned Circuits'. **Mullard Technical Communications,** Vol. 8, No. 78, Nov. 1965, pp. 249 to 255.
3. VENKATESWARAN, S., 'An Invariant Stability Factor and its Physical Significance'. **Proc. I.E.E.,** Part C, Vol. 109, No. 15, March 1962, pp. 98 to 102.
4. BUCKINGHAM, B. E., 'Determination of Stability Factor of a Four-terminal Network by Input Admittance Measurements'. **Mullard Technical Communications,** Vol. 8, No. 79, Jan. 1966, pp. 294 to 295.

Numerical Display with Cathode Ray Tube

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Central Application Laboratory, Philips, Eindhoven

A method of providing display of numerical data on a cathode ray tube screen is described. The circuit is given for a laboratory demonstration model which gives a fixed display of four rows of twelve characters. The principle used is that of a bar-matrix display which is selectively blanked or unblanked.

INTRODUCTION

This article describes a method of using a cathode ray tube to give instantaneous display of decimal numerical data which has been stored in a digital data processing system. Three main methods of achieving such a numerical display have been found to be practicable; these use either the Bar Matrix or a Dot Pattern or Lissajous Figures. The Bar Matrix method is used in the system described here. This method is very much easier than either of the other two methods to apply to cathode ray tubes which have electrostatic deflection, and, although the digits formed on the c.r.t. screen are not as well shaped as those in the other methods, they are nevertheless instantly recognisable and are easy to read accurately.

The laboratory model of this display unit uses the flat-faced mono-accelerator c.r.t. D10–16GH, which has a screen diameter of 10cm. The large display area (8cm × 6cm) and the small overall length (26cm) of this tube make it extremely suitable for incorporation into small desk-top calculators. If a larger display area is required, the c.r.t. D13–48GH may be used: this gives a display area of 10cm × 8cm and has an overall length of 31cm. For smaller display areas, the c.r.t. D7–19GH may be used to give a display area of 6cm × 5cm: the tube length is 21cm.

The system described in this article is designed to display 48 characters in four horizontal rows of twelve characters. Similar circuits using the same principle, however, may be designed to present either a larger number or a smaller number of characters. The laboratory model described is driven by a simple fixed pattern generator for demonstration purposes only: it can be adapted for displaying the output of any data handling system, provided that the input system and decoder still generate the necessary blanking signals for the z-amplifier.

The information to be displayed can be stored in any kind of memory circuit such as delay line, solid state or ferromagnetic. The store should be capable of being read out sequentially at sufficiently high speed to obviate perceptible flicker in the display: if N is the number of characters to be displayed, then the read-out speed must be at least (20 000/N)μs per character. That is, the memory must be capable of reading out all the relevant data in 20ms. The value of N in the circuit described is 48.

PRINCIPLE OF OPERATION

The block diagram of the display system is shown in Fig. 1. The generator for the basic figure 8 repeatedly causes the c.r.t. spot to trace out the rectilinear shape which is used to represent the character 8: a decimal point is included slightly to the right of this 8 pattern.

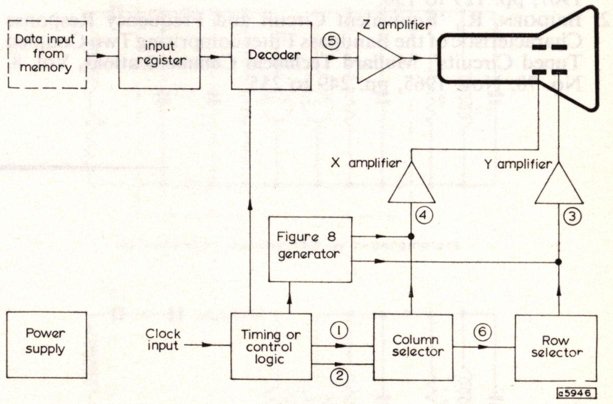

Data input from memory
Input register
Decoder
5
Z amplifier
X amplifier
Y amplifier
4
3
Figure 8 generator
Power supply
Clock input
Timing or control logic
1
2
Column selector
6
Row selector
a5946

Fig. 1—Block diagram of bar matrix numerical display system for c.r.t.

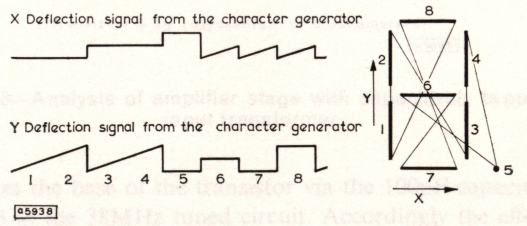

X Deflection signal from the character generator
Y Deflection signal from the character generator
1
2
3
4
5
6
7
8
Y
X
a5938

Fig. 2—Deflection signals from the figure 8 generator, and the basic figure 8 character

This pattern, and the waveforms which generate it, are shown in Fig. 2. The entire pattern is stepped to the right twelve times and traces twelve such characters in the top row. It is then stepped to the left position in the second row to begin the second row. Four rows are traced. The pattern produced would therefore be 48 identical characters all representing a figure 8 and a decimal point, except that nothing is visible on the c.r.t. screen because the spot is suppressed. However, parts of this pattern can be unblanked so that the unblanked portions display alternative characters as required. Those parts of the figure 8 which are to be unblanked and displayed to form the alternative characters are determined by the information decoder which applies appropriate signals via the z-amplifier to the grid of the c.r.t.

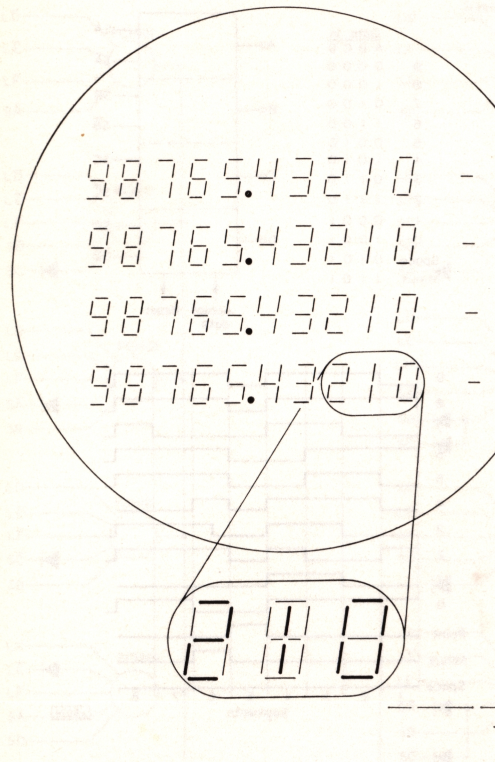

98765.43210 -
98765.43210 -
98765.43210 -
98765.43210 -
210

Fig. 3—Typical display of bar matrix numerals. This particular display is the one generated for demonstration purposes by the circuit described.

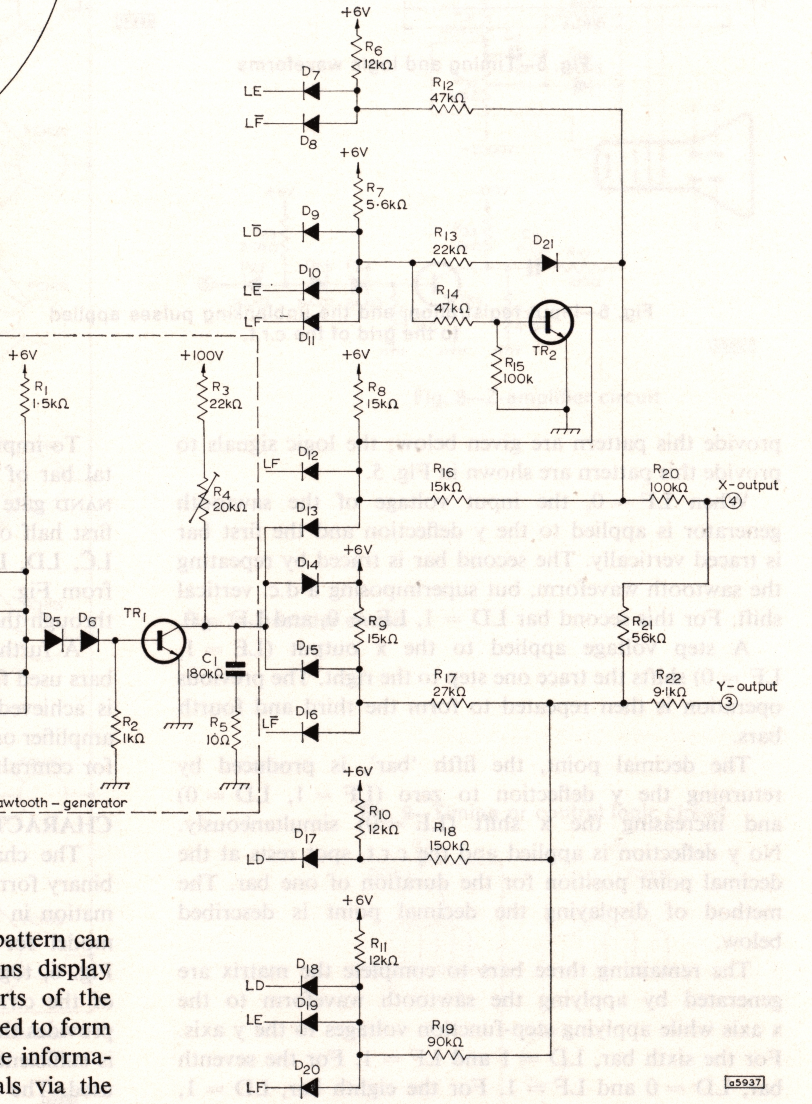

+6V
R6 12kΩ
D7
LE
LF
D8
R12 47kΩ
+6V
R7 5·6kΩ
D9
LD̄
R13 22kΩ
D21
D10
LĒ
LF
D11
R14 47kΩ
R15 100k
TR2
Clock
D1
LA
D2
D3
LB
D4
LC
D5
D6
TR1
+6V
R1 1·5kΩ
+100V
R3 22kΩ
R4 20kΩ
C1 180kΩ
R2 1kΩ
R5 10Ω
Sawtooth – generator
+6V
R8 15kΩ
D12
LF
D13
+6V
D14
R9 15kΩ
D15
D16
LF̄
R16 15kΩ
R20 100kΩ
X-output
4
R21 56kΩ
R17 27kΩ
R22 9·1kΩ
Y-output
3
+6V
R10 12kΩ
D17
LD
R18 150kΩ
+6V
R11 12kΩ
D18
LD
D19
LE
R19 90kΩ
D20
LF
a5937

Fig. 4—Pattern generator for the figure 8. Only one sawtooth generator is used. All transistors in this circuit are BSX20, and all diodes BAX13

Correct display of information demands that the correct synchronisation should always exist between the read-out, the pulses applied to the grid of the c.r.t., the generator producing the bar matrix figure 8 pattern, the row position selector and the column position selector. This synchronisation is provided by the timing or control logic circuit.

In this laboratory model, the entire screen display of 48 characters is covered in 12ms, and is therefore repeated slightly more than 80 times each second. This makes flicker imperceptible. The typical display shown in Fig. 3 is a fixed display, provided by the input registered decoder for demonstration purposes.

FIGURE 8 PATTERN GENERATOR

The bar matrix pattern formed by the figure 8 generator is shown in Fig. 2. The bars are traced in the order in which they are numbered. The c.r.t. spot rests in the fifth position for the time equal to the time used to trace a bar, and provides the decimal point. The circuit of the generator is shown in Fig. 4, and the logic inputs to the generator to

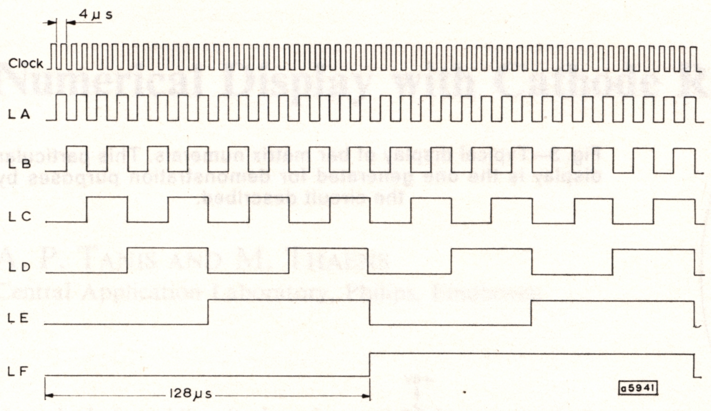


Fig. 5—Timing and logic waveforms

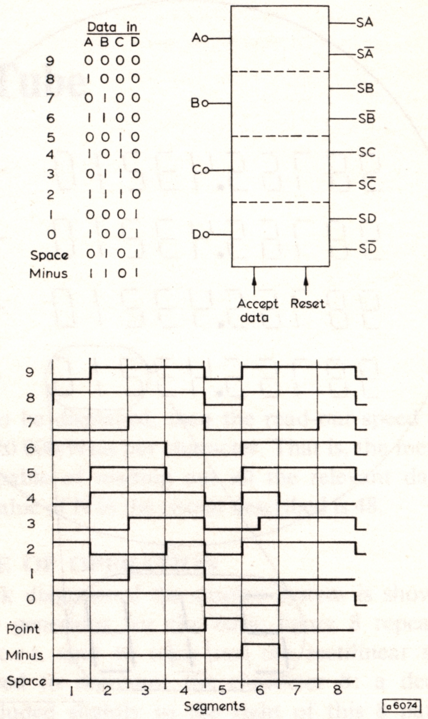

Data in
A B C D
9 0 0 0 0
8 1 0 0 0
7 0 1 0 0
6 1 1 0 0
5 0 0 1 0
4 1 0 1 0
3 0 1 1 0
2 1 1 1 0
1 0 0 0 1
0 1 0 0 1
Space 0 1 0 1
Minus 1 1 0 1
A
B
C
D
SA
SĀ
SB
SB̄
SC
SC̄
SD
SD̄
Accept data
Reset
9
8
7
6
5
4
3
2
1
0
Point
Minus
Space
1 2 3 4 5 6 7 8
Segments
a6074

Fig. 6—Input registration, and the unblanking pulses applied to the grid of the c.r.t.

provide this pattern are given below; the logic signals to provide this pattern are shown in Fig. 5.

When LF = 0, the input voltage of the sawtooth generator is applied to the y deflection and the first bar is traced vertically. The second bar is traced by repeating the sawtooth waveform, but superimposing a d.c. vertical shift. For this second bar LD = 1, LE = 0, and LF = 0.

A step voltage applied to the x output (LE = 1, LF = 0) shifts the trace one step to the right. The previous operation is then repeated to form the third and fourth bars.

The decimal point, the fifth 'bar', is produced by returning the y deflection to zero (LF = 1, LD = 0) and increasing the x shift (LE = 0) simultaneously. No y deflection is applied and the c.r.t. spot rests at the decimal point position for the duration of one bar. The method of displaying the decimal point is described below.

The remaining three bars to complete the matrix are generated by applying the sawtooth waveform to the x axis while applying step-function voltages to the y axis. For the sixth bar, LD = 1 and LF = 1. For the seventh bar, LD = 0 and LF = 1. For the eighth bar, LD = 1, LE = 1, and LF = 1.

With the method just described, the bar matrix generator requires only one sawtooth generating circuit. The procedure described, however, would generate an upright rectangular figure 8. A refinement is added that causes the pattern to be sloped slightly to the right at the top, increasing the legibility of the resulting characters. This is achieved by adding a small proportion of the y deflection to the x deflection. The resistor R_{21} in Fig. 4 is used to give the cross-coupling between the x and the y deflection to give the characters the appropriate slope.

To improve legibility, only half of the middle horizontal bar of the character 3 (sixth bar) is unblanked. The NAND gate FCH101 in the decoder circuit suppresses the first half of the bar. The necessary state of SA, SB, SC, L$\bar{C}$, LD, L$\bar{E}$, and LF to give this result can be derived from Fig. 5. It is the change of the state of LC halfway through the bar that provides the refinement.

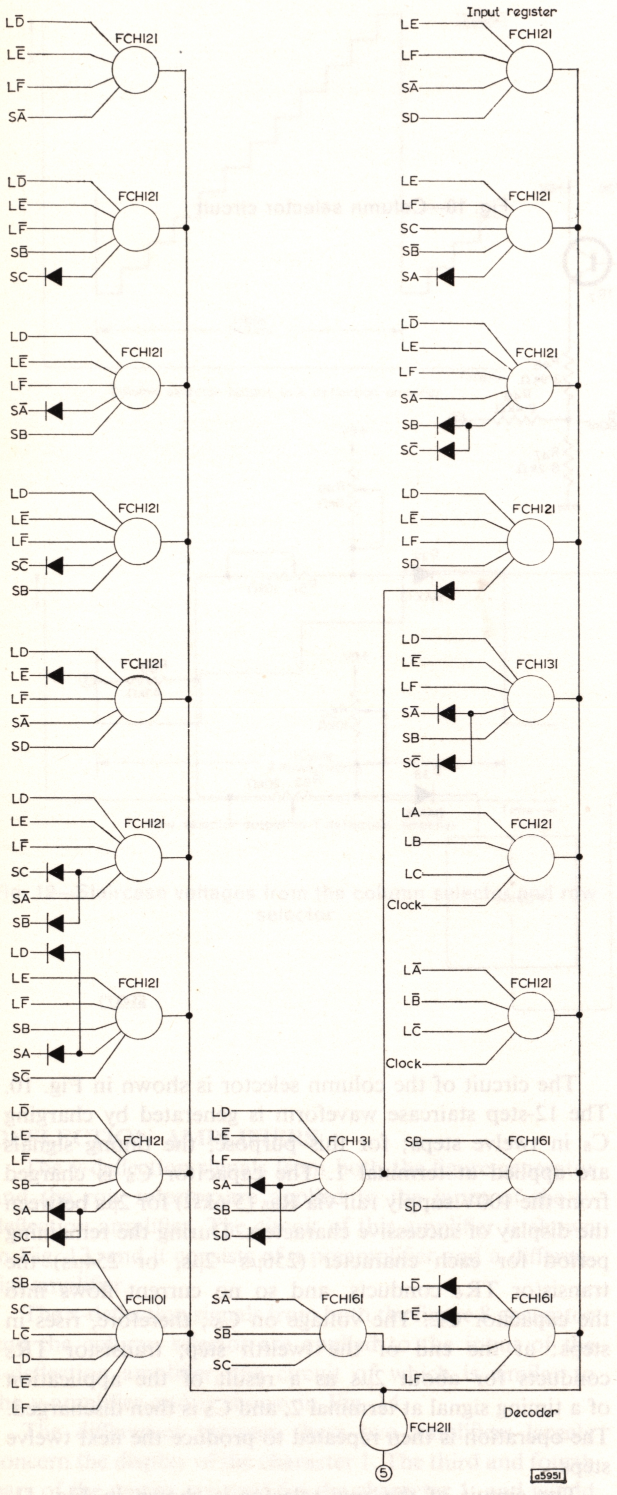
A further refinement is to centralise the two vertical bars used for displaying the character 1. The way that this is achieved is described under the description of the x-amplifier on page 205. A similar provision could be made for centralising the character 7.

CHARACTER SELECTION

The character to be displayed is presented in 4-bit binary form to the Input Register which stores the information in four flip-flop circuits. The coding used in this model for the twelve possible characters is shown in Fig. 6, together with the waveforms applied to the grid of the c.r.t. to provide each character. The z-amplifier provides these pulses at an amplitude of about 20V which is sufficient to unblank the beam of the c.r.t. in the tube used. The circuit of the decoder used for demonstration purposes, displaying exclusively the display shown in Fig. 3, is given in Fig. 7, and the circuit of the z-amplifier is given in Fig. 8. The decoder circuit must be adapted to suit the code being used in practice.

DISPLAY OF DECIMAL POINT

In the laboratory model described in this article, the decimal point is combined with the character 5, as can be seen from the fixed display in Fig. 3, but, in practice, the decimal point must be able to be placed in any position. This can be achieved by inserting an OR gate between


Input register
FCH121
FCH131
FCH161
FCH101
FCH211
Clock
Decoder
5
a5951

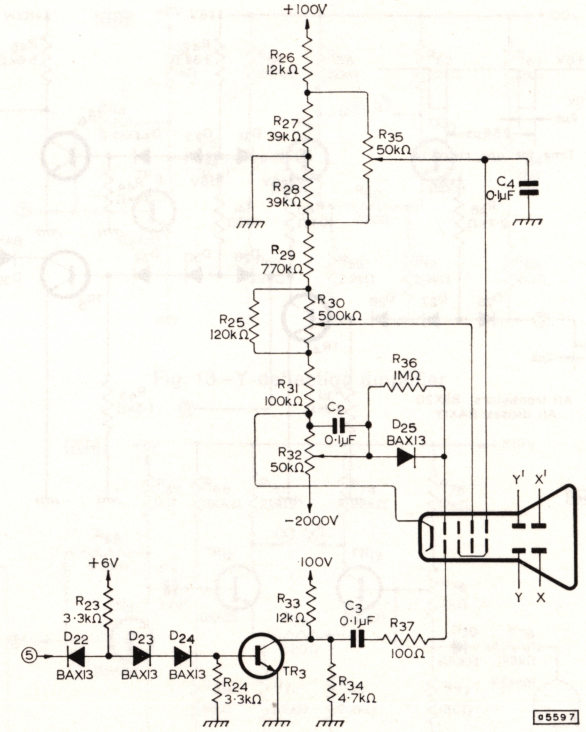
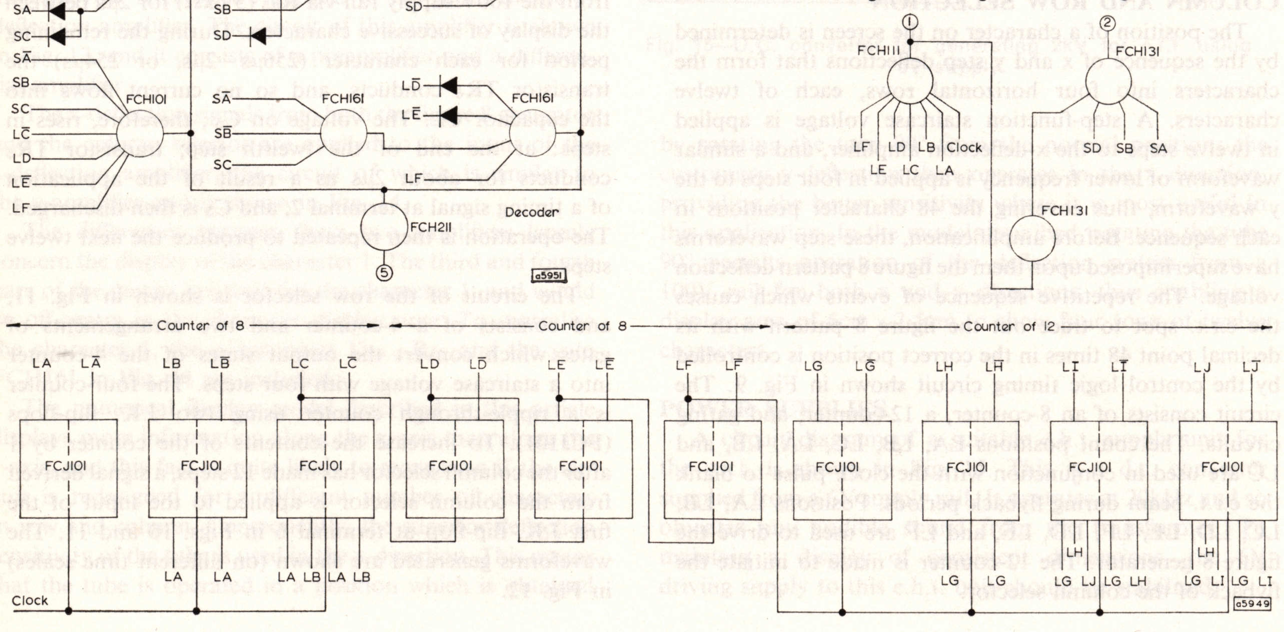

+100V
R26 12kΩ
R27 39kΩ
R28 39kΩ
R29 770kΩ
R30 500kΩ
R25 120kΩ
R31 100kΩ
R35 50kΩ
C4 0·1µF
R36 1MΩ
C2 0·1µF
D25 BAX13
R32 50kΩ
-2000V
Y' X'
Y X
+6V
R23 3·3kΩ
D22 BAX13
D23 BAX13
D24 BAX13
5
R24 3·3kΩ
TR3
100V
R33 12kΩ
C3 0·1µF
R37 100Ω
R34 4·7kΩ
a5597

Fig. 8—Z-amplifier circuit

Fig. 7—Decoder circuit

Fig. 9—Timing or control logic circuit


1
2
FCH111
FCH131
LF LD LB Clock
LE LC LA
SD SB SA
FCH131
Counter of 8
Counter of 8
Counter of 12
FCJ101
Clock
a5949

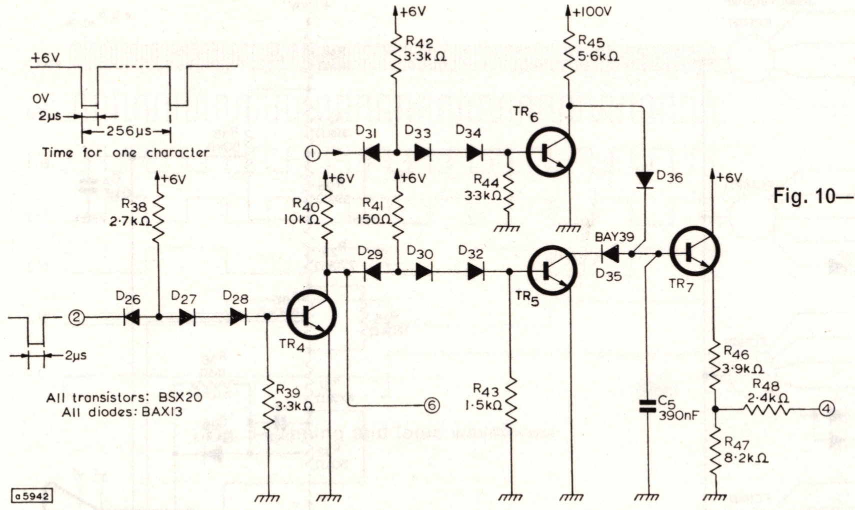

+6V
0V
2μs
256μs
Time for one character
+6V
R38 2·7kΩ
D26
D27
D28
2μs
TR4
R39 3·3kΩ
All transistors: BSX20
All diodes: BAX13
+6V
R42 3·3kΩ
+6V
R40 10kΩ
+6V
R41 150Ω
D31
D33
D34
D29
D30
D32
R44 33kΩ
R43 1·5kΩ
+100V
R45 5·6kΩ
TR6
TR5
D36
BAY39
D35
+6V
TR7
C5 390nF
R46 3·9kΩ
R48 2·4kΩ
R47 8·2kΩ
a5942

Fig. 10—Column selector circuit

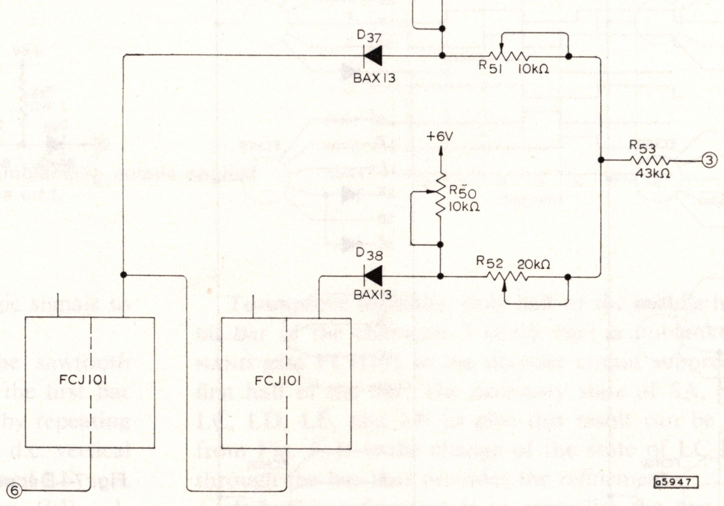

+6V
R49 5kΩ
D37
BAX13
R51 10kΩ
+6V
R50 10kΩ
R53 43kΩ
D38
BAX13
R52 20kΩ
FCJ101
FCJ101
a5947

Fig. 11—Row selector circuit

the decoder and the z-amplifier. One input of the OR gate should be driven by the appropriate signal from the data handling processor when the decimal point is required.

COLUMN AND ROW SELECTION

The position of a character on the screen is determined by the sequence of x and y step deflections that form the characters into four horizontal rows, each of twelve characters. A step-function staircase voltage is applied in twelve steps to the x-deflection amplifier, and a similar waveform of lower frequency is applied in four steps to the y waveform, thus covering the 48 character positions in each sequence. Before amplification, these step waveforms have superimposed upon them the figure 8 pattern deflection voltage. The repetitive sequence of events which causes the c.r.t. spot to trace out the figure 8 pattern with its decimal point 48 times in the correct position is controlled by the control logic timing circuit shown in Fig. 9. The circuit consists of an 8-counter, a 12-counter, and gating circuits. The count positions LA, LB, LC, LĀ, LB̄, and LC̄ are used in conjunction with the clock pulse to blank the c.r.t. beam during flyback periods. Positions LA, LB, LC, LD, LE, LF, LD̄, LĒ, and LF̄ are used to drive the figure 8 generator. The 12-counter is made to initiate the flyback of the column selector.

The circuit of the column selector is shown in Fig. 10. The 12-step staircase waveform is generated by charging C_5 in twelve steps; for this purpose, the timing signals are applied at terminal 1. The capacitor C_5 is charged from the 100V supply rail via R_{45} (5·6kΩ) for 2μs between the display of successive characters. During the remaining period for each character (256μs−2μs, or 254μs) the transistor TR_6 conducts, and so no current flows into the capacitor C_5. The voltage on C_5, therefore, rises in steps: at the end of the twelfth step, transistor TR_5 conducts for about 2μs as a result of the application of a timing signal at terminal 2, and C_5 is then discharged. The operation is then repeated to produce the next twelve steps.

The circuit of the row selector is shown in Fig. 11, and consists of a 4-counter and two arrangements of gates which convert the output states of the 4-counter into a staircase voltage with four steps. The four-counter is a ripple-through counter using two J.K. flip-flops (FCJ101). To increase the contents of the counter by 1 after the column selector has made 12 steps, a signal derived from the column selector is applied to the input of the first J.K. flip-flop at terminal 6 in Figs. 10 and 11. The waveforms generated are shown (on different time scales) in Fig. 12.

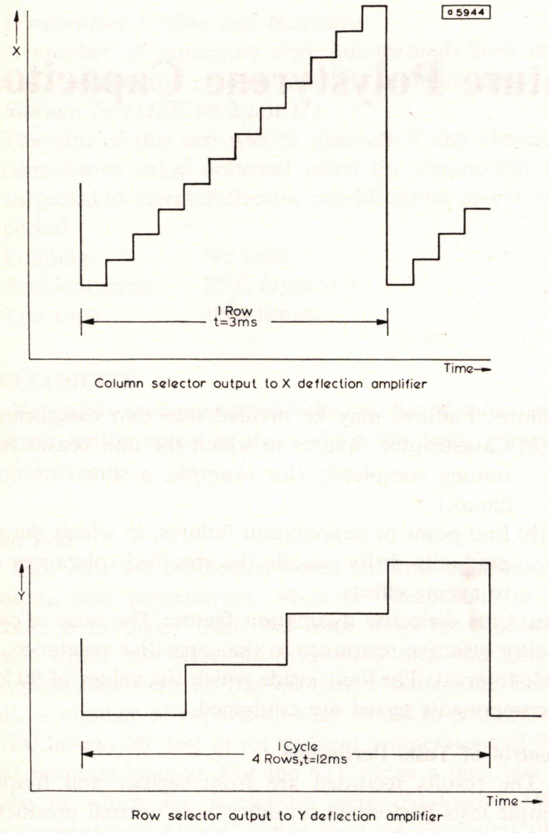


Fig. 12—Staircase voltages from the column selector and row selector

DEFLECTION AMPLIFIERS

The y-deflection signals from both the figure generator and the row selector are applied to the input of the y-deflection amplifier. The circuit of this amplifier is shown in Fig. 13, and it consists of a preamplifier and a differential amplifier.

The x-deflection signals from both the figure 8 generator and the column selector are applied to the input of the x-deflection amplifier, the circuit of which is similar to the y-amplifier and is shown in Fig. 14.

The differences between these two amplifiers largely concern the display of the character 1. The third and fourth bars of the matrix are used for the character 1, and would be off-centre in the character display area. To centralise the character 1, the components D_{39}, R_{78} and the gate FCH161 in Fig. 14 are included.

The numerical display model described in this article displays more information along the x-axis than along the y-axis, and this fact is quite likely to recur even if the circuit is redesigned for a different number of characters in row and column. Consequently, the superior deflection sensitivity of the tube is used in the x-direction. This means that the tube is operated in a position which is obtained by rotating the tube 90° from the normal position: the customary y-deflection then operates in the x direction, providing the better sensitivity where it is most useful in this application. In the model described, rotating the tube 90° permits operation of the deflection system from a 100V rail for both x and y directions, thus enabling a display area of 6cm×2·5cm to show four rows of twelve characters.

POWER SUPPLIES

A circuit diagram of a suitable e.h.t. supply unit for the c.r.t. is shown in Fig. 15. This is a d.c. converter supplied from a 6V supply rail. It operates at 20kHz and so obviates any audible sound from the transformer. To maintain a display of consistent dimensions, the 6V driving supply to this e.h.t. unit should be stabilised.

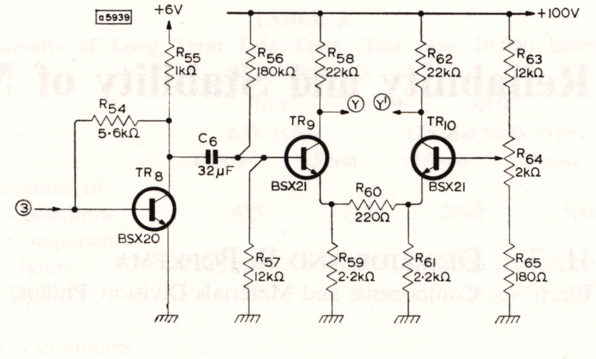

a5939
+6V
+100V
R55 1kΩ
R56 180kΩ
R58 22kΩ
R62 22kΩ
R63 12kΩ
R54 5·6kΩ
C6 32μF
TR8
TR9
TR10
Y
Y
BSX20
BSX21
BSX21
R60 220Ω
R64 2kΩ
R57 12kΩ
R59 2·2kΩ
R61 2·2kΩ
R65 180Ω

Fig. 13—Y-deflection amplifier

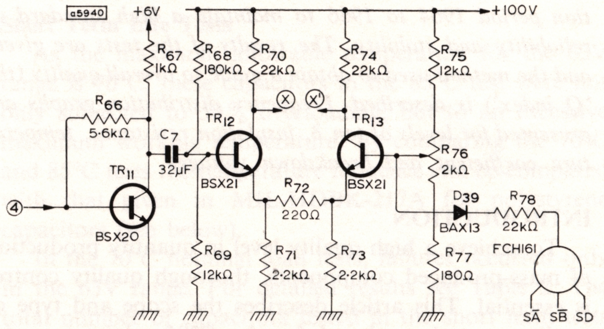

a5940
+6V
+100V
R67 1kΩ
R68 180kΩ
R70 22kΩ
R74 22kΩ
R75 12kΩ
R66 5·6kΩ
X
X
C7 32μF
TR11
TR12
TR13
BSX20
BSX21
BSX21
R72 220Ω
R76 2kΩ
D39
R78 22kΩ
BAX13
FCH161
R69 12kΩ
R71 2·2kΩ
R73 2·2kΩ
R77 180Ω
SA SB SD

Fig. 14—X-deflection amplifier

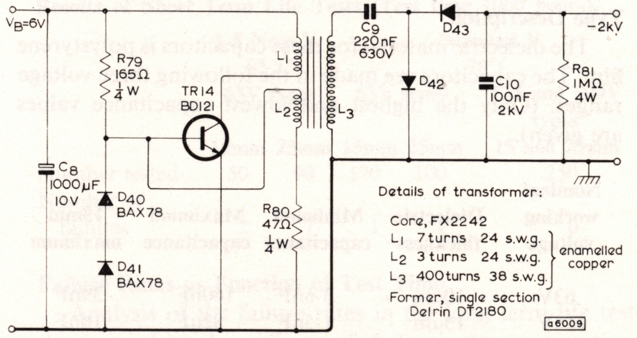

VB=6V
C9 220nF 630V
D43
−2kV
R79 165Ω ½W
L1
TR14 BD121
D42
C10 100nF 2kV
R81 1MΩ 4W
L2
L3
C8 1000μF 10V
D40 BAX78
R80 47Ω ¼W
D41 BAX78
Details of transformer:
Core, FX2242
L1 7 turns 24 s.w.g.
L2 3 turns 24 s.w.g.
L3 400 turns 38 s.w.g.
enamelled copper
Former, single section Delrin DT2180
a6009

Fig. 15—D.C. converter for generating 2kV for c.r.t. using 6V supply

Reliability and Stability of Miniature Polystyrene Capacitors

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This article describes the tests performed during the production period 1964 to 1966 to maintain a high standard of reliability and stability. The results of the tests are given, and the method used to obtain a guide to overall quality (the 'Q index') is described. Frequency distribution graphs are presented for levels of tan δ, insulation resistance, temperature coefficient and breakdown voltage.

INTRODUCTION

To achieve a high quality level in quantity production of mass-produced components, thorough quality control is essential. This article describes the scope and type of quality control employed for the C295 miniature polystyrene range of capacitors, and presents the results of tests carried out in the production period 1964 to 1966.

Type Description

The dielectric material for these capacitors is polystyrene film. The capacitors are made in the following three voltage ranges. (Only the highest and lowest capacitance values are given).

Nominal working voltage	Dielectric thickness	Minimum capacitance	Maximum capacitance	15mm maximum
63V	10μm	3·6nF	160nF	39nF
125V	15μm	1·5nF	82nF	16nF
500V	30μm	680pF	24nF	5·6nF

Two widths of polystyrene film were used to give two capacitor lengths: lower value capacitors with a length of 15mm and higher values with a length of 25mm. The highest capacitance values available in the 15mm range are shown in the last column.

Definitions

Confidence Level: The probability that a given statement is correct, or the chance that the true value lies between two confidence limits (the confidence interval). It is expressed as a percentage. For the failure rate calculations only the upper limit is given. For example, 60% confidence level means that the chance that the actual failure rate of the production will be better than indicated by the quality control tests, is 60%.

Failure: Failures may be divided into two categories:

(a) Catastrophic failures in which the unit ceases functioning completely (for example, a short- or open-circuit).

(b) End-point or degradation failures, in which the unit gradually drifts outside the specified tolerances due to ageing effects.

Tan δ, or dielectric dissipation factor: The ratio of capacitor effective resistance to the capacitive reactance.

90% Interval: The limit inside which the values of 90% of components tested are contained.

Control of Tests Performed

The results recorded are from regular and frequent sample tests performed on units from normal production in the period 1964 to 1966 inclusive. The tests were done in such a way that the results are representative of all values in the range during this production period.

Life tests were performed in accordance with IEC Specification 68-2.

Life Tests According to IEC 68-2, Test B.

This was a continuous loading test at a high temperature. Different test periods were used as follows:

Long Term Life Tests

Loading	1·5 × nominal d.c. voltage
Ambient temp.	85°C (for 63V range, at 70°C)
Test time	10 000 hours

Short Term Life Tests

Loading	Nominal d.c. voltage
Ambient temp.	70°C
Test time	1000 hours

For the 63V range only:

Loading	1·5 × nominal d.c. voltage
Ambient temp.	85°C
Test time	1000 hours.

Climatic Tests

Temperature Cycling test (IEC 68-2 test N).

The capacitors were kept, without load, at 85°C for 3 hours (63V range, 70°C), followed by a 3-hour period at −40°C.

Humidity Test (IEC 68-2 test C)

The capacitors were exposed to a high relative humidity at a moderate temperature.

Loading	No load
Ambient temp.	40°C
Rel. humidity	90 to 95%
Test time	56 days

The information contained herein is in close accordance with the IEC publication IEC56 (Central Office) 8: 'Presentation of Reliability Data on Electronic Components (or Parts)', January 1967.

Temperature Cycling and Humidity

A number of capacitors were put through both tests: first, temperature cycling, then the humidity test.

Storage Test (IEC 68-2 test H)

The aim of this test was to discover if any change in capacitance value occurred when the component was subjected to 'normal' climatic conditions for an extended period.

Loading	No load
Ambient temp.	25°C (approx.)
Test time	4000 hours.

RELIABILITY

Reliability is connected with the number of catastrophic failures which occur in the various life tests, expressed as failure rates.

Life Tests

Life tests are performed under extreme conditions of loading and temperature. Most of the results in this article were taken from the long term (10 000 hours) tests, where the overload was 50% and the ambient temperatures were at the maximum allowable. Besides this, a number of capacitors were tested in a short term (1000 hours) life test at an ambient temperature of 70°C and nominal loading. For the 63V range a final test was done in which the capacitors were overloaded (50%) at a temperature 15degC higher than the maximum allowable.

Failure rates were expressed in failures per million hours in accordance with MIL-HDBK-217A. The failure rates are specified for a confidence level of 60%. To ensure this degree of confidence, it becomes necessary to add a certain number of failures to the number actually observed, thus artificially raising the failure rate. This additional number is represented by B_{60} in the expression used to determine failure rates, as follows:

$$FR_{60} = \frac{\text{Number of failures} + B_{60}}{\text{Number of component-hours}}.$$

The failure rate calculated in this way gives an averaged figure for all values in the production range during the total test period, for the conditions specified in the test. The resulting failure rates are then further analysed, and if some relation between the failure rate and one of the parameters is found, it is mentioned.

Long Term Life Tests

Table 1 gives a summary of the results obtained. These tests were performed at an overload of 50% and maximum allowable ambient temperature: 70°C for the 63V range, 85°C for the other ragnes. The total test time was 10 000 hours. In total, 3170 capacitors were tested, giving 24 170 000 component hours.

The 63V range clearly has a higher failure rate, despite the lower maximum temperature. The failure rates for the 25mm ranges are over four times those for the 15mm ranges.

The results for the separate 125V and 500V ranges are not detailed as there were no clear differences observable between them.

TABLE 1

Results of Long Term Life Tests (Test time 10 000 hours, 50% overload).

	70°C		85°C	
	63V types		125 and 500V types	
	15mm	25mm	15mm	25mm
Number of Capacitors	475	155	2040	500
Component hours	2 615 000	475 000	17 640 000	3 440 000
Failures	13	11	34	27
FR in failures per million hours (Confidence level 60%)	5·6	26·4	2·0	8·1

Short Term Life Tests

As the maximum allowable temperature for the 63V range is 70°C, these capacitors in the 85°C test were not only subjected to 50% overloading, but to an excessive maximum working temperature. By comparing the 70°C and 85°C tests the temperature influence can be compared with that given in MIL-HDBK-217A for polystyrene capacitors (see below).

In the 70°C nominal load tests, failures occurred only in the 63V range. For detailed results see Table 2. The total number of capacitors tested in the short term tests is too small to provide a reliable figure for the failure rates.

TABLE 2

Results of Short Term Life Tests (Test time 1000 hours).

	1·5 Nom.V		Nominal V		
	85°C		70°C		
	63V types		63V types		125 and 500V types
	15mm	25mm	15mm	25mm	15 and 25mm
Number tested	50	90	170	100	250
Number of failures	2	7	1	1	0

Failure Rates as Function of Test Time

Analysis of the failure rates in the long term life tests shows a clear dependence of failure rate on test time. The values given in Table 1 must thus only be taken as averages during the first 10 000 hours. Fig. 1 gives the failure rate at each moment within the 10 000 hour test period for each capacitor type.

These graphs clearly show the differing ways in which the failure rates for the various types change during the test period. In the period considered, only the 15mm

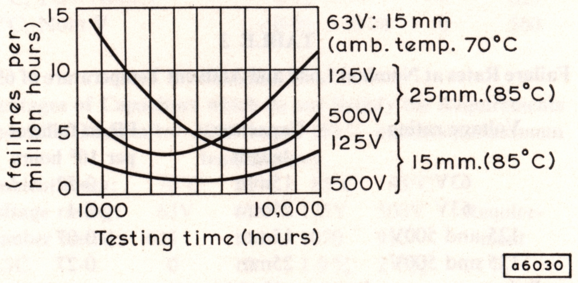

Fig. 1—Failure rate as function of testing time for different capacitor ratings

version of the 125V and 500V types has a fairly constant failure rate.

Comparison with MIL-HDBK-217A

MIL-HDBK-217A gives failure rates for polystyrene capacitors at various loadings and temperatures. Fig. 2 is a copy of the Standard. It may be seen that only nominal load and a maximum temperature of 65°C are used.

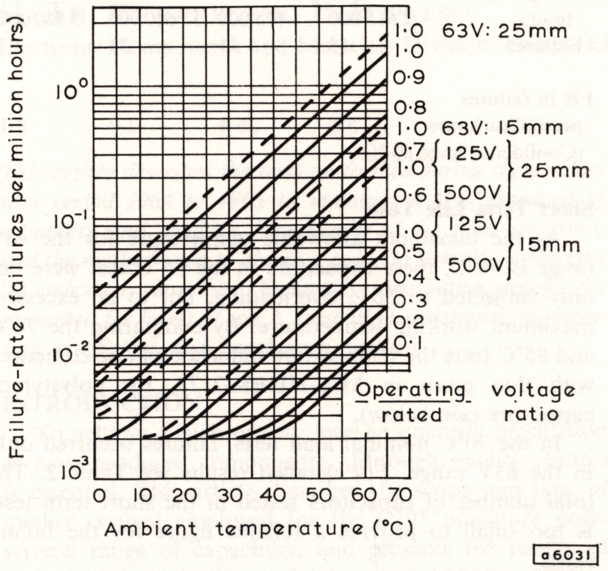

Fig. 2—Comparison of MIL-HDBK-217A failure rate specification (Polystyrene Capacitors MIL-C-19978) with miniature polystyrene capacitor failure rates

Since the failure rates in this article are for 50% overload and 85°C (70°C for 63V range), they are not directly comparable with the MIL standard.

From the information given in Fig. 2 it can be deduced that:

(i) The failure rate increases with the fifth power of the voltage increase (at a higher loading than 0·5 times nominal).

(ii) A temperature rise of 10degC doubles the failure rate.

If these 'accelerating factors' are also applicable to our miniature polystyrene capacitors, the failure rates should be appreciably lower at *nominal* loading and ambient temperatures of 65°C, by factors of:

63V range: $1{\cdot}5^5 \times 2\ exp\ (70-65)/10 = 10{\cdot}7$

125 and 500V ranges: $1{\cdot}5^5 \times 2\ exp\ (85-65)/10 = 30{\cdot}4$

Table 3 gives the failure rates at nominal loading and 65°C which were calculated from the above factors.

For comparison, the failure rate lines for the different miniature capacitor types are drawn in Fig. 2.

TABLE 3

Failure Rates at Nominal Load and Ambient Temperature of 65°C·

Voltage rating	Capacitor length	FR in failures per 10^6 hours
63V	15mm	0·52
63V	25mm	2·4
125 and 500V	15mm	0·07
125 and 500V	25mm	0·27
Polystyrene capacitors specified in MIL-HDBK-217A		1·8

Failure Rates under Derated Conditions

With the 'accelerating factors' obtained from MIL-HDBK-217A (Fig. 2) it is also possible to make an estimation of the failure rate under derated conditions (using the information given in Table 1).

The large amount of extrapolation needed to obtain the derated failure rates means that only coarse estimates can be given. Table 4 is only intended to permit comparison with field data (where derating is often used).

To improve readability of these very small values, a unit of 10^{-9} instead of 10^{-6} has been chosen.

TABLE 4

Failure Rates under Derated Conditions

		Failure rates	
Nominal voltage	Length	0·5×Nom.V 50°C	0·5×Nom.V 25°C
63V	15mm	6×10^{-9}	1×10^{-9}
63V	25mm	30×10^{-9}	5×10^{-9}
125V and 500V	15mm	1×10^{-9}	$0{\cdot}15\times10^{-9}$
125V and 500V	25mm	3×10^{-9}	$0{\cdot}5\times10^{-9}$

The above figures agree quite well with information from Bell Telephone Laboratories* and CNET Centre de Fiabilité for capacitors having polystyrene as the dielectric:

Bell Laboratories (recommended for use in computers):	5×10^{-9}
CNET Centre de Fiabilité (from experience):	14×10^{-9}

Failure Rate as a Function of Ambient Temperature

It was assumed that the acceleration factor of 2 per 10degC for our capacitors was the same as found from the MIL-HDBK-217A specification. This can be checked by conducting two endurance tests on the 63V range at differing ambient temperatures and the same loading.

The results from the first 1000 hours of the test at 70°C gave failure rates of 25 and $6{\cdot}5\times10^{-6}$ for the 25mm and 15mm versions respectively. With a factor of 2 per 10degC, the failure rates should be, for 85°C:

Failure rate $= \{2\ exp\ (85-70)/10\}\times25\times10^{-6}$
$= 71\times10^{-6}$ for the 63V, 25mm version.

Failure rate $= \{2\ exp\ (85-70)/10\}\times6{\cdot}5\times10^{-6}$
$= 18\times10^{-6}$ for the 63V, 15mm version.

For the number of capacitors tested at 85°C (90 and 50 respectively), the following number of failures should be expected:

63V, 25mm type: $71\times10^{-6}\times90\times10^3 = 6{\cdot}4$ failures.

63V, 15mm type: $18\times10^{-6}\times50\times10^3 = 0{\cdot}9$ failures.

These expected numbers of failures agree quite well with the actual numbers, which were 7 and 2 respectively. This shows that the temperature dependence factor for capacitors of this type is indeed about 2 per 10degC.

Failure Rate as a Function of Production Period

To conclude, a review is given of the influence of manufacturing improvements on the failure rate level.

During production, continual attempts are made to improve the average quality and to eliminate variations. The way in which these improvements have affected the failure rate levels is shown in Fig. 3, where the 500V, 15mm type has been used as the most typical example. For this type results were available on production back to the year 1963, in addition to the figures given in this article (from January 1964). Fig. 3 shows the failure rate as a function of the testing time for various production periods.

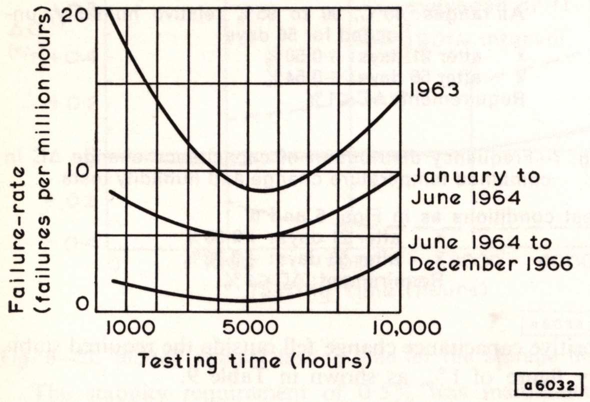

Fig. 3—Failure rate as function of testing time for different production periods

The number of capacitors tested in each period was as follows:

Production period 1963:	210
January to June 1964:	200
July 1964 to Dec. 1966:	540

The bottom curve is the *averaged* failure rate for the production period on which this article is based. As the three curves indicate a definite decrease of failure rate, it may be expected that 1966 was an improvement on 1964, and that further improvements will take place in the future.

Climatic Tests

In all, 4890 capacitors were subjected to climatic tests. They were divided into groups as shown in Table 5.

TABLE 5

Numbers Tested in Climatic Tests

Voltage rating:	63V	125V	500V	Total
Temp. change test (3h at +85°C; 3h at −40°C)	240	675	900	1815
Humidity test (40°C; 90 to 95% R.H., 56 days)	135	1030	1400	2565
Temp. change followed by humidity	75	80	100	255
Shelf life test (25°C, 4000 hours)	75	80	100	255

No catastrophic failures occurred in any of the 4890 capacitors tested. This means that the average percentage of failures is less than 0·02%, for a confidence level of 60%.

STABILITY

After discussion and presentation of figures giving the percentage of capacitors which do not satisfy specification, graphical information is displayed on average values and drift of nominal capacitance for the various tests:

Life tests – the above is done for the averaged capacitance value and the 90% interval, as a function of time.

Climatic tests – for these tests frequency distributions of the change in capacitance are given.

Stability During Life

A complete review of stability in the long-term life tests is given in Fig. 4. Here the averaged capacitance drift and the 90% interval are given as a function of the test time (up to 10 000 hours).

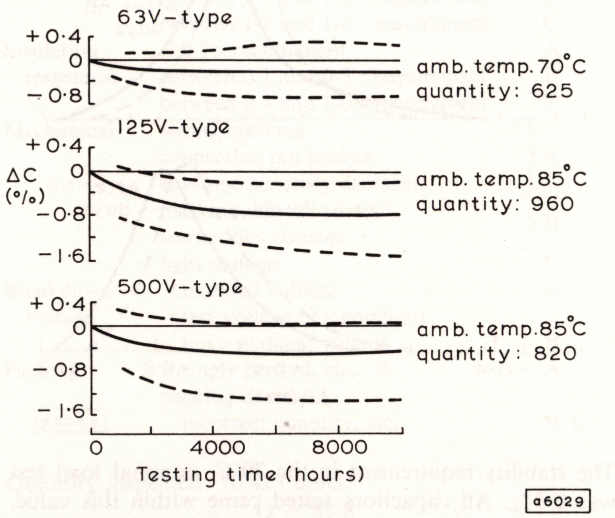

Fig. 4—Capacitance change (drift) as a function of testing time for each voltage rating

From the capacitors tested at 85°C, 50% overload for 10 000 hours, the type with the higher voltage rating showed, despite the higher field strength, a smaller capacitance drift, as follows:

125V type, −0·84% 500V type, −0·55%.

The averaged capacitance drift was not clearly dependent on the nominal capacitance value.

The small capacitance change of the 63V type showed that the temperature has a large influence on the stability. On comparing the average change after 1000 hours for the various types (see Table 6), it may be seen that the stability at an ambient temperature of 70°C and at nominal load is considerably better for all types.

TABLE 6

Averaged Percentage Capacitance Change in the Various Life Tests after 1000 Hours Testing Time.

Voltage rating:	63V	125V	500V	Number tested
85°C, 1·5×Nom.V	−0·20	−0·38	−0·25	2680
70°C, 1·5×Nom.V	−0·12	—	—	625
70°C, Nom.V	−0·01	−0·06	0	560

TABLE 7

Percentages of Capacitors which do not Satisfy the Requirements of the Life Tests after 1000 hours (50% overload, maximum temperature)

Ambient temp:	70°C	85°C	85°C	85°C	
Voltage rating:	63V	63V	125V	500V	Requirement
Number tested:	625	140	1070	910	
ΔC	0	0	1·9%	2·7%	≤1%
tan δ	0	0	0	0	$\leqslant 3\times10^{-4}$
Ins. res.	0	0	0·2%	0	$\geqslant 10^6$MΩ

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*'Operational Reliability of Components in Selected Systems', T. L. James, Bell Telephone Laboratories, U.S.A.

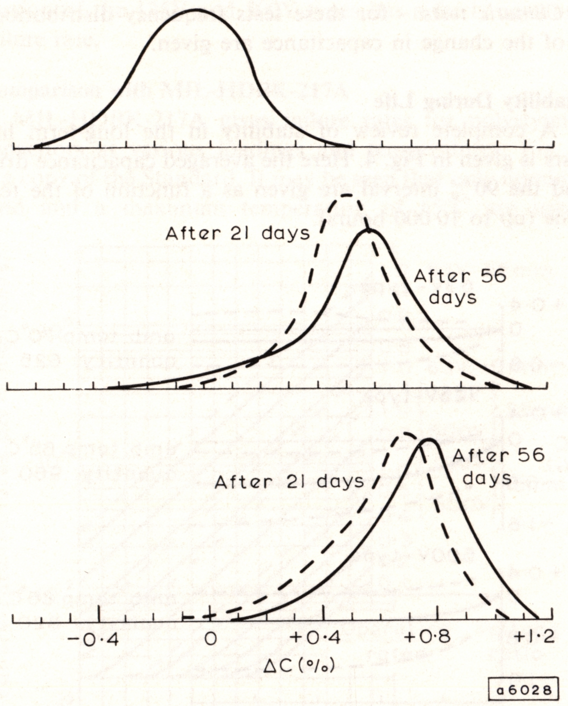

Fig. 5—Frequency distribution of capacitance change ΔC in temperature cycling tests

63V range: 3h at +70°C, 3h at −40°C
All other types: 3h at +85°C, 3h at −40°C
$\bar{x} = -0{\cdot}09$
Requirement: $\Delta C \leqslant 0{\cdot}5\%$

Fig. 6—Frequency distribution of capacitance change ΔC in humidity test

All ranges: 40°C, 90 to 95% relative humidity, unloaded for 56 days
$\bar{x}$ after 21 days: +0·50%
$\bar{x}$ after 56 days: +0·54%
Requirement: $\Delta C \leqslant 1\%$

Fig. 7—Frequency distribution of capacitance change ΔC in combined temperature change and humidity tests

Test conditions as in Figs. 5 and 6
$\bar{x}$ after 21 days: +0·60%
$\bar{x}$ after 56 days: +0·72%
Requirement: $\Delta C \leqslant 1\%$

The stability requirement in the 70°C, nominal load test was 0·5%. All capacitors tested came within this value. From the overload tests, the percentages by which the specified limiting values are exceeded were determined, as shown in Table 7.

Stability in Climatic Tests

Figs. 5 to 7 show frequency distributions for capacitance change in the climatic tests (except for the storage test). These distributions are valid for all voltage ratings, since there was no difference in capacitance drift between the various ratings.

Temperature Cycling Test

The averaged capacitance change appears to be quite small, and negative. The spread, however, is substantial. From the frequency distribution it may be seen, however, that only a small percentage do not satisfy the stability requirement of 0·5%. Table 8 also gives the percentages of capacitors which do not satisfy the requirements for tan δ and insulation resistance after the test.

TABLE 8

Percentages of Capacitors which do not Satisfy the Requirements of the Temperature Cycling Test

Voltage rating:	63V	125V	500V	**Required**
Number tested:	240	675	550	**value**
ΔC	0·8	2·8	2	$\leqslant 0{\cdot}5\%$
tan δ	0	0	0	$\leqslant 3 \times 10^{-4}$
Ins. res.	0·4	0·15	0	$\geqslant 10^{-6}$MΩ

Humidity Test

For this test measurements were made after 21 days and after 56 days. The capacitance change was positive, as shown in Fig. 6, and took place mainly within the first 21 days. Only the spread of the capacitance change clearly increased between 21 and 56 days. A small percentage with positive capacitance change fell outside the required stability figure of 1%, as shown in Table 9.

TABLE 9

Percentages of Capacitors which do not Satisfy the Requirements of the Humindity Test.

Voltage rating:	63V	125V	500V	**Required**
Number tested:	125	1030	840	**value**
ΔC	1·5	1·2	2·3	$\leqslant 1\%$
tan δ	0	0	0	$\leqslant 5 \times 10^{-4}$
Ins. res.	8	0·2	0·1	$\geqslant 10^{4}$MΩ

Temperature Change and Humidity Tests

As both the previous climatic tests are combined for this test, it would be expected that the total capacitance change is the sum of the changes previously found. The averaged change is, however, greater than this, as shown in Fig. 7. The influence of a humidity test is thus greater if large temperature changes occur before the humidity test is carried out. This can be explained by the fact that the large temperature changes cause such a mechanical strain on the encapsulation of the capacitor that the component becomes less protected against humidity.

Since, however, the same stability requirement ($\leqslant 1\%$) is imposed as for the humidity test alone, it must then be expected that the percentage of components which do not satisfy the specified requirements will be greater. In Table 10 this does not appear to be so (probably because of the small number tested).

TABLE 10

Percentages of Capacitors which do not Satisfy the Requirements for Temperature Cycling and Humidity Tests.

Voltage rating:	63V	125V	500V	**Required**
Number tested:	75	80	65	**value**
ΔC	1·3	1·5	1·5	$\leqslant 1\%$
tan δ	0	0	0	$\leqslant 5 \times 10^{-4}$
Ins. res.	5·3	2·3	1·5	$\geqslant 10^{4}$MΩ

Storage Test

Fig. 8 gives the averaged capacitance change and the 90% interval as a function of test time.

In this graph the averaged capacitance change is seen to be very small. The width of the 90% interval increases, however, from 0·4% at 1000 hours to approx. 0·7% at 4000 hours.

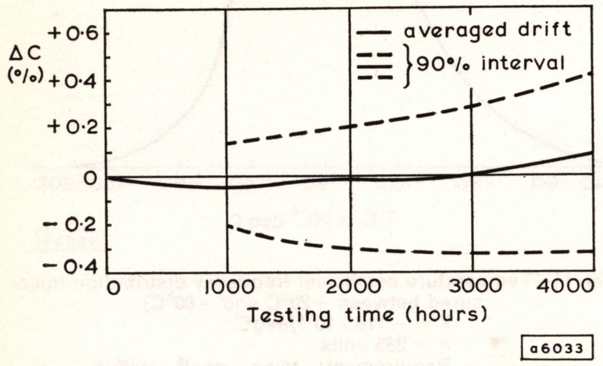

Fig. 8—ΔC plotted against testing time for the storage test

The stability requirement of 0·5% was maintained. At 1000 hours and 2000 hours, no capacitors were found to exceed the requirements. At 4000 hours, only four capacitors out of the total of 255 were found to have a capacitance change greater than the 1000-hour requirement (0·6, 0·7, 0·8 and 1% change).

THE Q INDEX; RESULTS OF FAULT CLASSIFICATION TESTS

As a final check on the manufacturing process a 100% inspection is made on the main capacitor properties: capacitance value, tan δ, and breakdown voltage. After this 100% test a sample test is made to determine the quality level of the finished product. This sample test includes, in addition to the above-mentioned main properties, a check on insulation resistance, mechanical damage, and packaging. The sample test is done in such a way that it is representative of the whole production.

Each departure from specification is categorised as follows, in accordance with Table 11:

'A' fault – this is so serious that correct working of the apparatus is endangered.

'B' fault – under certain conditions difficulties could be expected.

'C' fault – not a serious departure from the specification.

Each 'A' fault is given a value of 100 penalty points, 'B' faults 10 penalty points, and 'C' faults 1 penalty point. From the total number of penalty points and the total number of capacitors inspected, the Q index is calculated. The following formula is used:

$$Q = 100 - 100 \times \frac{\text{Number of penalty points}}{\text{Quantity inspected}}.$$

The results of the inspections are regularly discussed with the production staff. In these discussions, the way the various factors affect the Q index obtained are considered. In addition, by comparing the Q indices obtained in previous periods, a guide is formed as to future improvement or deterioration of the quality. The results of inspections in the two months October and November 1966 are given below.

TABLE 11

Extract from the Inspection List for Miniature Polystyrene Capacitors

Property	**Departure from optimum condition**	**Fault type**
Capacitance	>1·5×tolerance	A
	between 1·5 and 1·2×tolerance	B
	between 1·2 and 1·0×tolerance	C
tan δ	>1·5×requirement	A
	between 1·5 and 1·2×requirement	B
	between 1·2 and 1·0×requirement	C
Insulation resistance	<0·1×requirement	A
	between 0·1 and 0·5×requirement	B
	between 0·5 and 1·0×requirement	C
Mechanical	wrong marking	A
	connection pin broken	
	envelope seriously damaged	
	marking difficult to read	B
	less serious damage	
	light damage	C
Breakdown voltage	<nominal voltage	A
	<test voltage (2×nominal) but>nominal voltage	B
Packing	wrongly packed, etc.	A
	packing damaged, incorrect quantity, etc.	B, C

Quantity inspected: 70 413 units

Q = 87·8.

Analysis of points lost (total 12·2):

1·2 points: Capacitance values outside tolerance

0·1 points: Breakdown voltage between 1 and 2 times nominal voltage

2·2 points: Marking incorrect

8·7 points: Departures from the standard mechanical properties.

LEVELS OF SOME IMPORTANT PROPERTIES

Accurate measurements are performed on a smaller number of capacitors than used for determination of the Q index, for the following properties: tan δ, insulation resistance, temperature coefficient, and breakdown voltage.

These measurements form part of the normal quality control process and thus enable unfavourable departures from the standard properties to be quickly observed, before the limiting requirement is exceeded. In this way it is also possible to obtain information about the actual values of the various properties.

Figs. 9 to 12 give a complete picture of the form and spread of the properties mentioned above.

Tan δ. (Fig. 9) conforms completely to the requirement.

The RC product for all capacitance values is the same. The frequency distribution (Fig. 10) therefore gives a picture of the average and spread of the RC product for the various ratings and capacitance values. The specified requirement is for insulation resistance only, given for capacitance values of above and below 100nF. Since the insulation resistance is inversely proportional to the capacitance value, it is preferable to make the insulation resistance requirement linearly dependent on the capacitance; that is, to have a single value for the RC product.

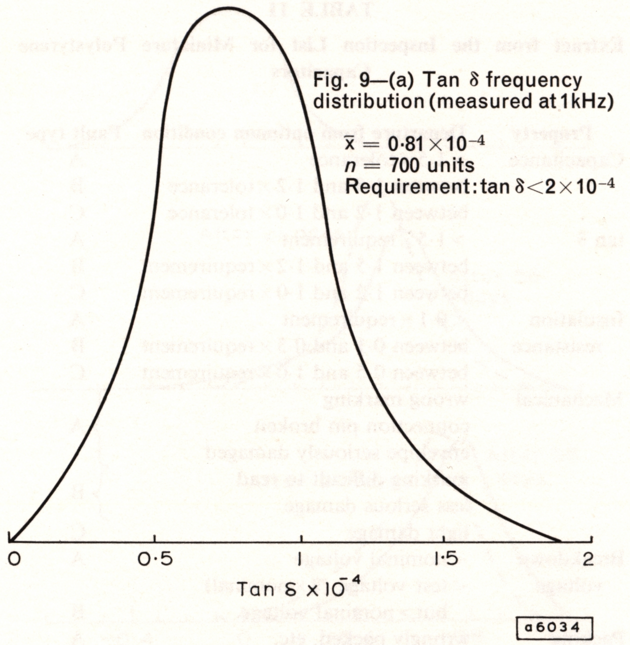

Fig. 9—(a) Tan δ frequency distribution (measured at 1kHz)
$\bar{x} = 0{\cdot}81\times10^{-4}$
$n = 700$ units
Requirement: tan $\delta<2\times10^{-4}$

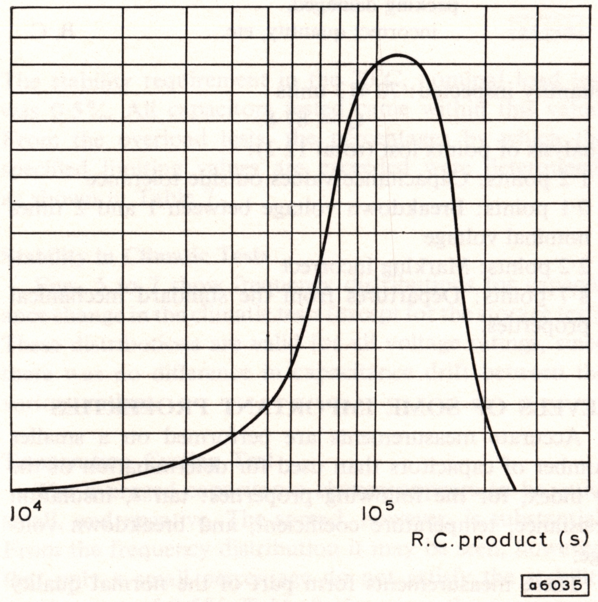

Fig. 10—RC product frequency distribution
$\bar{x} = 1{\cdot}3\times10^5$ sec.
$n = 1250$ units
Requirement for insulation resistance:
$\geqslant$100nF, 10^{5}MΩ
$<$100nF, 10^{6}MΩ

The requirement for temperature coefficient (-100 ± 50) $\times10^{-6}$/degC, was not wholly satisfied (Fig. 11). About 4% of the measured capacitors had a temperature coefficient lying outside the -150×10^{-6}/degC limit.

The frequency distribution of the breakdown voltage of the various voltage ratings is given (Fig. 12) as a function of the dielectric thickness. Here, the average breakdown voltage (dependent on the type) was from 6 to 20 times as high as the nominal voltage. The 125V rating type has the most efficient dielectric thickness (15μm). The value of volts per μm is less at both thicker and thinner dielectric thickness (see table 12).

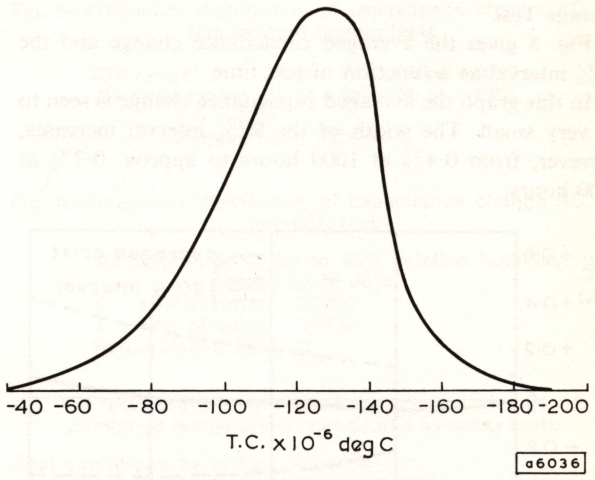

Fig. 11—Temperature coefficient frequency distribution (measured between +20°C and +80°C)
$\bar{x} = -118\times10^{-6}$/degC
$n = 235$ units
Requirement: temp. coeff. within $-(100\pm50)\times10^{-6}$/degC

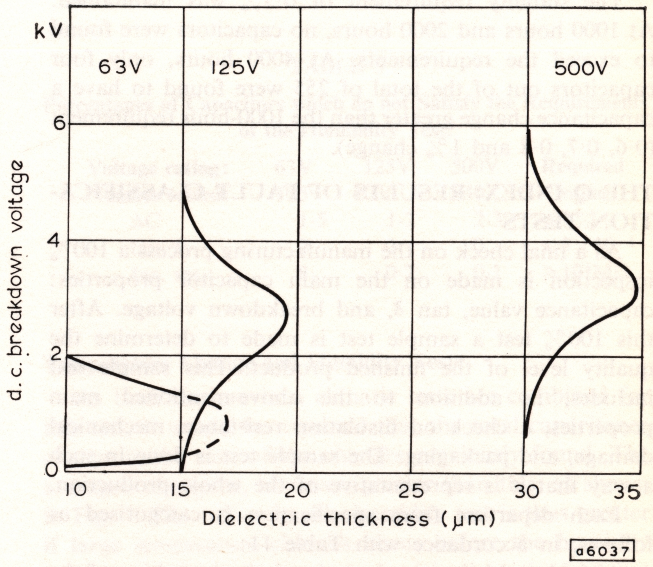

Fig. 12—Breakdown voltage frequency distribution for three different dielectric thicknesses

Nom. voltage,	$V_{d.c.}$	63	125	500
$\bar{x}$	$V_{d.c.}$	800	2500	3200
n	units	130	825	530
Requirement	$V_{d.c.}$	125	250	1000

The requirement for breakdown voltage is a minimum of twice the nominal voltage. All 1485 capacitors tested conformed to this requirement.

TABLE 12

Averaged Breakdown Voltages and Volts per μm of the Various Voltage Ratings.

Voltage Rating	Dielectric thickness in μm	Averaged breakdown voltage	Volts per μm
63V	10	800$V_{d.c.}$	80
125V	15	2500$V_{d.c.}$	167
500V	30	3200$V_{d.c.}$	107